

## PCN Product/Process Change Notification

### Additional Assembly and Test Location in China for Protection devices housed in SMA / SMB packages

<b>Notification number:</b>	IPD-DIS/9053	<b>Issue Date</b>	03/02/2015
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<b>Issued by</b>	Aline AUGIS
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<b>Product series affected by the change</b>	The <b>product series</b> involved in this production extension are listed below.			
	SMB unidirectionnel	SMB bidirectionnel	SMA unidirectionnel	SMA bidirectionnel
	SM6T15A	SM6T15CA	SMAJ12A-TR	SMAJ12CA-TR
	SM6T18A	SM6T18CA	SMAJ13A-TR	SMAJ13CA-TR
	SM6T22A	SM6T22CA	SMAJ15A-TR	SMAJ15CA-TR
	SM6T24A	SM6T24CA	SMAJ18A-TR	SMAJ18CA-TR
	SM6T27A	SM6T27CA	SMAJ20A-TR	SMAJ24CA-TR
	SM6T30A	SM6T30CA	SMAJ24A-TR	SMAJ26CA-TR
	SM6T33A	SM6T33CA	SMAJ26A-TR	SMAJ28CA-TR
	SM6T36A	SM6T36CA	SMAJ28A-TR	SMAJ30CA-TR
	SM6T39A	SM6T39CA	SMAJ30A-TR	SMAJ33CA-TR
	SMBJ12A-TR	SM6T56CA	SMAJ33A-TR	SMAJ40CA-TR
	SMBJ15A-TR	SM6T68CA		SMAJ43CA-TR
	SMBJ16A-TR	SMBJ12CA-TR		SMAJ48CA-TR
	SMBJ18A-TR	SMBJ13CA-TR		SMAJ58CA-TR
	SMBJ20A-TR	SMBJ15CA-TR		SMAJ70CA-TR
	SMBJ22A-TR	SMBJ18CA-TR		
	SMBJ24A-TR	SMBJ20CA-TR		
	SMBJ26A-TR	SMBJ22CA-TR		
	SMBJ28A-TR	SMBJ24CA-TR		
	SMBJ30A-TR	SMBJ26CA-TR		
	SMBJ33A-TR	SMBJ28CA-TR		
		SMBJ30CA-TR		
		SMBJ33CA-TR		
	SMBJ36CA-TR			
	SMBJ40CA-TR			
	SMBJ48CA-TR			
	SMBJ58CA-TR			
	SMBJ70CA-TR			

<b>Type of change</b>	Assembly site multisourcing
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**Description of the change**  
 In order to better meet the market demand, we have decided to **expand our manufacturing capacities** for all our **Protection devices** housed in **SMA / SMB package** with one **additional assembly and test line** in a new **China subcontractor**.

Multi-sourcing	Package	Current	New
Assembly & test location	SMA / SMB	CHINA (subco 1) – ECOPACK@2 MOROCCO (ST plant) – ECOPACK@2	CHINA (subco 1) – ECOPACK@2 MOROCCO (ST plant) – ECOPACK@2 CHINA (subco 2) – ECOPACK@2

**Specific devices** not expressly listed in the above table are included in this change.

(1) IPD: Industrial & Power Discretes - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

**Reason for change**

This multi-sourcing will increase our **manufacturing capacity** for a better service on the considered **Protection devices** housed in the **SMA / SMB** package.

**Former versus changed product:**

The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet

The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged.

The footprint recommended by ST remains the same.

There is no change in the packing modes and the standard delivery quantities either.

The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

**Disposition of former products**

Deliveries of former product will continue.

**Marking and traceability**

**Traceability** for the implemented change will be ensured by the **marking**, an **internal codification** and by the **Q.A. number**.

Package	Marking
MOROCCO (ST plant)	CZ
CHINA (subco 1)	GP
CHINA (subco 2)	G3

**Qualification complete date**

22-05-2014

**Forecasted sample availability**

Samples are available upon request.

**Change implementation schedule**

Sales types	Estimated production start	Estimated first shipments
All	W22-2014	W19-2015

**Comments:**

**Customer’s feedback**

Please contact your local ST sales representative or quality contact for requests concerning this change notification.  
 Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change  
 Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

**Qualification program and results**

QRP14107 Attached

## Reliability Report

*Additional Assembly and Test Location in China  
for protection devices in SMA / SMB packages*

General Information																																																																																																																	
<b>Product Line</b>	<i>Protection / Transil standard</i>																																																																																																																
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<b>Package</b>	<i>SMA / SMB</i>																																																																																																																
<b>Maturity level</b>	<i>Qualified</i>																																																																																																																

Locations	
<b>Wafer fab</b>	<i>ST TOURS (FRANCE)</i>
<b>Assembly plant</b>	<i>ST CHINA</i>
<b>Reliability Lab</b>	<i>ST TOURS (FRANCE)</i>

### DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	13/01/2015	7	J.MICHELON	J.P. REBRASSE	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.  
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## **1 APPLICABLE AND REFERENCE DOCUMENTS**

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP 2614	Reliability requirements for product qualification
0061692	Reliability tests and criteria for qualifications
SOP 2610	general product qualification procedure
JESD 22	Reliability test methods for packaged devices

## **2 GLOSSARY**

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size
PC	Pre-conditionning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
uHAST	Unbiased Highly Accelerated Stress Test
THB	Temperature Humidity Bias

## **3 OBJECTIVES**

### **Reason for the change:**

This multi-sourcing will increase our manufacturing capacity for a better service on the considered Protection devices housed in the SMA / SMB package.

## **4 CONCLUSION**

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

## 5 DEVICE CHARACTERISTICS

### 5.1 Description of the change

In order to better meet the market demand, we have decided to expand our manufacturing capacities for all our Protection devices housed in SMA / SMB package with one additional assembly and test line in a new China subcontractor.

Multi-sourcing	Package	Current	New
Assembly & test location	SMA / SMB	CHINA (subco 1) – ECOPACK®2 MOROCCO (ST plant) – ECOPACK®2	CHINA (subco 1) – ECOPACK®2 MOROCCO (ST plant) – ECOPACK®2 <b>CHINA (subco 2) – ECOPACK®2</b>

Specific devices not expressly listed in the above table are included in this change.

## 6 TESTS RESULTS SUMMARY

### 6.1 Test vehicle

Lot #	Commercial product	Wafer manufacturing plant	Assembly plant	Comments
Lot 1	SMAJ33CA	STMicroelectronics Tours (France)	CHINA subcon 2	Qualification lots
Lot 2	SMAJ70CA			
Lot 3	SMBJ70CA			
Lot 4	SMAJ12A			
Lot 5	SMAJ33A			
Lot 6	SMBJ70A			

## 6.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS						Note
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	
<b>Package Oriented Tests</b>												
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85% Bias = VRM	100	168h	-	0/25	0/25	-	-	0/25	
					504h	-	0/25	0/25	-	-	0/25	
					1000h	-	0/25	0/25	-	-	0/25	
TC	Y	JESD22 A-104	-65°C/+150°C 2 cycles/hour	100	100C	-	0/25	0/25	-	-	0/25	
					500C	-	0/25	0/25	-	-	0/25	
uHAST	Y	JESD22 A-102	T=130°C RH=85%, P=2.3 Bars	100	96h	-	0/25	0/25	-	-	0/25	
Repetitive surges	Y	ADCS0060 282	Ipp <sub>max</sub> datasheet	140	140	0/20	0/20	0/20	0/20	0/20	0/20	
Solderability	N	JESD22 B-102	Dry ageing 16h SnPb bath and SnAgCu Wet ageing 8h SnPb bath and SnAgCu	60	Visual inspection	-	-	-	0/60	-	-	
<b>Die Oriented Tests</b>												
HTRB	N	JESD22 A-108	Tj = 150°C, Bias = VRM	385	168h	0/77	0/77	0/77	0/77	0/77	-	
					504h	0/77	0/77	0/77	0/77	0/77	-	
					1000h	0/77	0/77	0/77	0/77	0/77	-	

### 6.3 Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTRB</b> High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
<b>Package Oriented</b>		
<b>uHAST</b> Unbiased Highly Accelerated Stress Test	The device is stored without bias under 130°C 85% RH during 96 hours, or equivalent 110°C 85% RH during 264 hours.	The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion).
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
<b>THB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.



Test name	Description	Purpose
<p><b>TC</b> Temperature Cycling</p>	<p>The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.</p>	<p>To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.</p>
<p><b>Solderability</b></p>	<p>The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.</p>	<p>This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.</p>
<p><b>Repetitive surges</b></p>	<p>Devices are submitted to rated Ipp for 50 surges.</p>	<p>This test is intended to verify robustness of device submitted to rated Ipp (as per data sheet) = exploration of reverse characteristic at a calibrated current value followed by the measure of voltage clamping value. Failure mode expected is short circuit of the device due to hot spot creation into silicon bulk at device periphery where the electrical field gradient is the most important. Physical analysis must be done to verify consistency of the failure mode and discriminate from extrinsic causes related to process escapes.</p>