



**PRODUCT/PROCESS
CHANGE NOTIFICATION
PCN 10816 – Additional information**

**TSMC (Taiwan) additional source
for STM32F4 & STM32F7 listed products
in M10/90nm technology**

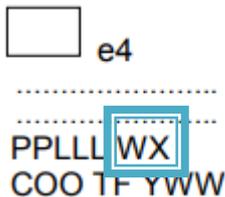
MDG - Microcontrollers Division (MCD)

Fab 14 TSMC is a fab already diffusing 90nm used for STM32L4 products.

Design database remains the same, except few changes on dummy structures at mask level to adapt to fab equipment.

How can the change be seen?

The standard marking is:



WX code indicates the diffusion traceability plant code.

Please refer to the DataSheet for marking details.

The marking is changing as follows:

Existing		Additional	
WX code	Fab	WX code	Fab
VQ	ST Crolles CR300 (France)	9R	TSMC Fab14 (Taiwan)



MCU DIVISION NOTE – October 30th, 2017

M10/90nm Additional Front-end Source

MMS - Microcontrollers Division (MCD)

Dear Customer,

We are in the process to transfer ST M10/90nm eNVM technology, currently used to produce our STM32F2x, STM32F4x and STM32F7x product to TSMC Fab 14 located in Taiwan. Fab14 is currently producing STM32L4x products.

Most of the STM32F2x, STM32F4x and STM32F7x volume production will be transferred to TSMC Fab 14.

This letter is a pre-announcement. Formal PCN will follow in coming weeks.

Why to add a source for M10 technology

- STM32F2x, STM32F4x and STM32F7x are experimenting a big success in the market and we are facing a growing and solid demand since months.
- Our two production sites ST Rousset R8 and ST Crolles CR300 fabs will not be able to absorb all future demand. Adding TSMC Fab14 as manufacturing source will provide the flexibility to cope with future demand and further growth.

Products involved

- STM32F2x
- STM32F4x
- STM32F7x

Timing:

- We intend to complete qualification of all part number by Q3 2018.
- First PCN announcing the first part number batch of transfer will be published mid-November 2017 for delivery starting in March 2018.
- ST will do its best to support customers during the short transition time.

Sincere regards.

Veronique Barlatier
WW Commercial Marketing Manager
ST Microcontroller Division



RER1715

for PCN10333, PCN10544, PCN10595, PCN10703,
PCN10596, PCN10671 & PCN10816

TSMC Taiwan Fab14 additional source for STM32
products in M10/90nm technology

Reliability Evaluation Plan

June 13rd, 2018

MMS MCD Quality & Reliability Department



RER1715 TSMC Fab14 for STM32 products in M10/90nm technology

STM32 Die Test Vehicles

Die Vehicle	Process Perimeter	Assembly Line	Package	Number of Reliability Lots
413	M10	ATP3	UFBGA10*10 176b	3 lots to qualify Process Perimeter Then 1 lot by Die
411		ATP3	UFBGA10*10 176b	
419		ATP3	TFBGA13*13 216b	
449		ATP3	TFBGA13*13 216b	
458	M10 ULP	JSCC	LQFP10*10 64L	3 lots to qualify Process Perimeter Then 1 lot by Die
423		ATP1	LQFP14*14 100L	
431		ATP1	LQFP14*14 100L	
441		ATP3	UFBGA10*10 144b	
433		ATP1	LQFP14*14 100L	
421		ATP1	UFBGA7*7 144b	
452		ATP3	UFBGA10*10 176b	
463		ATP3	UFBGA10*10 144b	
434		ATP3	TFBGA13*13 216b	
451		ATP3	TFBGA13*13 216b	

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STM32 Die Reliability Trials

Reliability Trial & Standard		Test Conditions	Pass Criteria	Lot Strategy	Units per Lot
ESD HBM	0060102 JESD22-A114ANSI/ESDA JEDEC JS-001	25°C	2kV (class 2)	1 to 3 lots	3
ESD CDM	ESD Charged Device Model ANSI/ESD STM5.3.1	Aligned with device datasheet	250V to 500V	1 lot	3
LU	0018695 JESD78	125°C REG-ON Configuration 125°C REG-OFF Configuration	No concern	1 to 3 lots	3 3
EDR + Bake	JESD22-A117 JESD22-A103	125°C & 3.6V Cycling 150°C Bake	10k cycles 1500h 1000h	1 to 3 lots 1 st lot 2 nd & 3 rd if any	77
EDR + Bake	JESD22-A117 JESD22-A103	25°C & 3.6V Cycling 150°C Bake	10k cycles 168h	1 to 3 lots	77
EDR + Bake	JESD22-A117 JESD22-A103	-40°C & 3.6V Cycling 150°C Bake	10k cycles 168h	1 to 3 lots	77
ELFR	MIL-STD-883 Method 1005 JESD22-A108 JESD74	125°C & 3.6V	48h	3 lots by process perimeter	500 units min per lot Total of 2000 units
HTOL	MIL-STD-883 Method 1005 JESD22-A108	125°C & 3.6V 100MHz	1200h 600h	1 st lot 2 nd & 3 rd if any	77

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STM32 Package Test Vehicles

Package Line	Assembly Line	Package	Wire	Die Vehicle / Rawline (*)	Number of Reliability Lots
LQFP	ATP1	LQFP10*10 64L	Au	413 / 5W*413	3 lots to qualify M10 Technology Then 1 lot by Package Assembly Line
	JSCC	LQFP10*10 64L	Ag	413 / 5W*413	
	ATP1	LQFP14*14 100L	Au	431 / 1L*431	
	ATP1	LQFP20*20 144L	Au	413 / 1A*413	
	ASE	LQFP24*24 176L	Au	413 / 1T*413	
	ATP1	LQFP28*28 208L	Au	419 / UH*419	
QFN	JSCC	UQFN7*7 48L	Ag	458 / MI*458	
UFBGA	ATP3	UFBGA10*10 176b	Au	413 / MR*413	
TFBGA	ATP3	TFBGA8*8 100b	Au	449 / DY*449	
	ATP3	TFBGA13*13 216b	Au	419 / RM*419	
WLCSP	ATT1	WLCSP 36b	NA	458 / 8Q*458	
	ATT1	WLCSP 90b	NA	413 / RI*413	
	ATT1	WLCSP 143b	NA	419 / VH*419	
	ATT1	WLCSP 180b	NA	451 / 8Z*451	

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STM32 Package Reliability Trials

Reliability Trial & Standard		Test Conditions	Pass Criteria	Lot Strategy	Units per Lot
PC	Pre Conditioning: Moisture Sensitivity Jedec Level 1 or 3 J-STD-020/ JESD22-A113	Bake (125°C / 24h) Soak (85°C / 85% RH / 168h) for level 1 Soak (30°C / 60% RH / 192h) for level 3 Convection reflow: 3 passes	3 Passes	1 to 3 lots	231 to 308 (**)
UHASt (*) (**)	Unbiased Highly Accelerated Temperature & Humidity Stress JESD22-A118	130°C, 85%RH, 2 Atm	96h	1 to 3 lots	77
TC (*)	Thermal Cycling JESD22-A104	-65°C +150°C	500Cy	1 to 3 lots	77
THB (*)	Temperature Humidity Bias JESD22-A101	85°C, 85% RH, bias	1000h	1 to 3 lots	77
HTSL (*)	High Temperature Storage Life JESD22-A103	150°C - no bias	1000h	1 to 3 lots	77
Construction Analysis	JESD22-B102	Including Solderability & Physical Dimensions	No concern	1 by package assembly line	15
	JESD22-B100/B108				10
ESD CDM	ESD Charged Device Model ANSI/ESD STM5.3.1	Aligned with device datasheet	250V to 500V	1 by package assembly line	3

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