PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/18/10777

Analog & MEMS Group (AMS)

Qualification of ST Shenzhen as Assembly and Test & Finishing site for selected products of General Purpose Analog and Industrial & Power Conversion Divisions in SO16 package

WHAT:

Progressing on activities related to production rationalization and capacity increase, ST is pleased to announce the qualification of some IPC (Industrial & Power Conversion) and GPA (General Purpose Analog) products in ST Shenzhen.

Please find more information related to the transfer of the impacted products:

Material	Current process	Modified process	Comment
Diffusion location	No change		No change
Assembly location	ST Bouskoura Amkor Philippines (TSM104)	ST Shenzhen Amkor Philippines (TSM104)	
Test location	ST Bouskoura	ST Shenzhen	
Molding compound	Hitachi MP8000 Sumitomo G700K (ST8034)	Sumitomo G630AY	No change for TSM104
Die attach	HITACHI EN4900 ST10 ABLESTIK 8601S-25 (ST8034)	ABLESTIK 8601S-25	No change for TSM104
Lead frame	Copper 85x85mils(ST8034) Copper 94x125 Copper 94x160 (TSM102)	Copper 94x150 Copper 94x200 (TSM102)	No change for TSM104
Wire	Gold wire 1mil Copper wire 1 mil (ST8034)	Copper wire 1 mil	No change for TSM104
Plating	Preplated e4		No change
MSL	No change		No change

Samples of vehicle test are available now and other samples will be launched upon customer's re-quests. Please submit requests for samples within 30 days of this notification.

WHY:

The purpose of the transfer is to rationalize our production tool and increase capacity.

HOW:

•The qualification is based on representative Test vehicles, using internal ST rules for changes.
•To validate the change, dedicated engineering trials have been performed and reliability report is attached.

IMPACTS OF THE CHANGE:

Form/Fit/Fonction : No change

WHEN:

For all impacted products, estimated 1st shipment start date is wk35 2018.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.
There is -as well- no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

Shipments may start earlier with the customer's written agreement.

STMicroelectronics
Manufactured under patents or patents pending
Assembled in: COUNTRY
PbFree Second level interconnect
MSL: X Bag sealed date: XX XXX XXXX
PBT: XXX°C Catergory: ECOPACK/Rohs
TYPE Commercial product
Finished good
Total Qty: XXXX
Trace codes PPYWWLLL WX TF
PPYWWLLL WX TF
PPYWWLLL WX TF
Marking MARKING
Bulk Id Number
Bar code
Please provide the bulk Id for any inquiry

On tracecode "PP" code will move from "CZ" (ST Bouskoura) to "GK" (ST Shenzhen)

Reliability Report

Qualification of ST Shenzhen as Assembly and Test & Finishing site for selected products of GPA and IPC Divisions in SO16 package

General Information	
Product Line	*UI87, 0102, UW55*
Product Description	16-pin smartcard interfaces, VOLTAGE AND CURRENT CONTROLLER, 3 to 5.5 V, low-power, up to 400 kbs RS-232 drivers and receivers,
P/N	ST8034TDT, TSM102/A, ST3232B
Product Group	*AMS*
Product division	*General Purpose Analog &RF, Industrial Power Conversion*
Package	*SO16*
Silicon Process technology	*BCD6S, Bipolar, BCD3S,*

Locations	
Wafer fab	*ST Singapore, ST Agrate, ST Catania*
Assembly plant	*ST Shenzhen*
Reliability Lab	*ST Grenoble, ST Casteletto, ST Catania ST Shenzhen*

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
0061692	Reliability tests and criteria for qualifications

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify SO16 package in ST Shenzhen for General purpose analog and Industrial & Power Conversion products.

3.2 Conclusion

Qualification Plan requirements will have to be fulfilled without issue. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

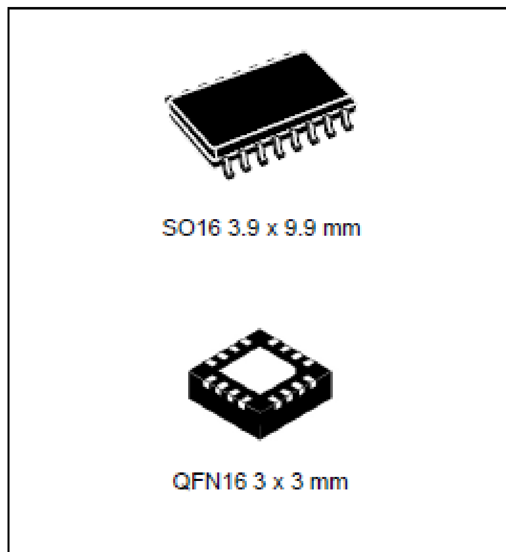
4 DEVICE CHARACTERISTICS

4.1 Device description

ST8034T, ST8034AT, ST8034P, ST8034C

16-pin smartcard interfaces

Datasheet - production data



SO16 3.9 x 9.9 mm

QFN16 3 x 3 mm

Features

- Complete smartcard interface
- ISO 7816 and EMV™ 4.3 payment systems compatible
- One protected half-duplex bidirectional buffered I/O line to the smartcard
- 5 V or 3 V (or 1.8 V in case of ST8034P) selectable smartcard supply voltage (V_{CC}). Ensures controlled V_{CC} rise and fall times and provides smart overload detection with glitch immunity.
- Optional chip select function allows the device interface to be isolated from the host microcontroller signals - allows parallel combination of the card interface devices (ST8034C)
- Card clock generation by integrated crystal oscillator or from external clock source
- Card clock frequency up to 20 MHz, programmable by CLKDIV pin, with synchronous frequency changes
- Optional VCC_SEL input for pin-controlled selection of V_{CC}; 5 V or 3 V or 1.8 V (ST8034P)
- Automatic card activation and deactivation sequences initiated by the microcontroller
- Emergency deactivation sequences initiated by a card supply short-circuit, card take-off, falling V_{DD}, V_{DDP}, or $V_{DD(INTF)}$ or by the interface device overheating
- Voltage supply supervisors
  - With a fixed threshold (V_{DD}, V_{DDP}, and $V_{DD(INTF)}$)
  - Optionally with an external resistor divider to set the $V_{DD(INTF)}$ threshold (PORADJ pin; ST8034P and ST8034C)
- Multipurpose card status signal $\overline{OFF}$
- Non-inverted card reset pin RST driven by the RSTIN input
- Thermal and short-circuit protection of all card contacts
- Card presence detection contacts debounced
- Enhanced card side ESD protection of 8 kV
- Common SO16 3.9 x 9.9 mm body or a space-saving QFN16 3 x 3 mm package
- Temperature range -25 to +85 °C

Applications

Smartcard readers for

- Set-top boxes
- Pay-TV
- Identification
- Banking
- Tachographs

TSM102/A

VOLTAGE AND CURRENT CONTROLLER

OPERATIONAL AMPLIFIERS

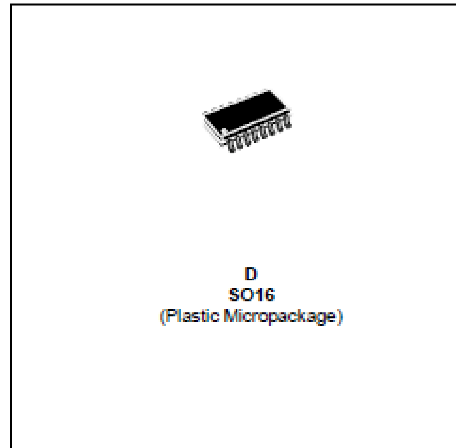
- LOW SUPPLY CURRENT : 200µA/amp.
- MEDIUM SPEED : 2.1MHz
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^- : 0.1V typ.
- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND

COMPARATORS

- LOW SUPPLY CURRENT : 200µA/amp.
- (V_{CC} = 5V)
- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250mV (Io = 4mA)

REFERENCE

- ADJUSTABLE OUTPUT VOLTAGE :
- V_{ref} to 36V
- SINK CURRENT CAPABILITY : 1 to 100mA
- 1% and 0.4% VOLTAGE PRECISION
- LACTH-UP IMMUNITY



D
SO16
(Plastic Micropackage)

DESCRIPTION

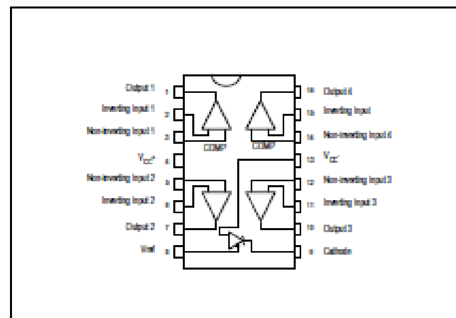
The TSM102 is a monolithic IC that includes two op-amps, two comparators and a precision voltage reference. This device is offering space and cost saving in many applications like power supply management or data acquisition systems.

ORDER CODE

Part Number	Temperature Range	Package
		D
TSM102I	-40°C, +85°C	•
TSM102AI	-40°C, +85°C	•

D = Small Outline Package (SO) - also available in Tape & Reel (DT)

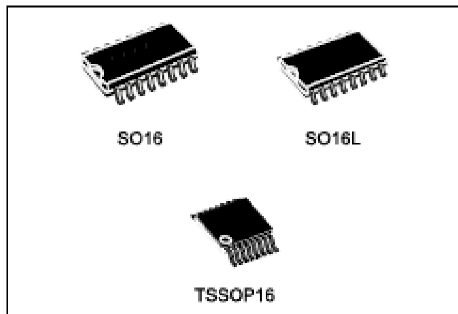
PIN CONNECTIONS (top view)



ST3232B, ST3232C

3 to 5.5 V, low-power, up to 400 kbs RS-232 drivers and receivers

Datasheet - production data



Features

- 300 µA supply current
- 300 kbps minimum guaranteed data rate
- 6 V/µs minimum guaranteed slew rate
- Meets EIA/TIA-232 specifications down to 3 V
- Available in SO16, SO16L, and TSSOP16 packages

Description

The ST3232B and ST3232C devices are 3 V powered EIA/TIA-232 and V.28/V.24 communication interfaces with low power requirements and high data-rate capabilities.

These devices have a proprietary low dropout transmitter output stage providing true RS-232 performance from 3 to 5.5 V supplies. The devices require only four small 0.1 mF standard external capacitors for operation from a 3 V supply.

The ST3232B and ST3232C have two receivers and two drivers.

The devices are guaranteed to run at data rates of 250 kbps while maintaining RS-232 output levels. Typical applications are notebooks, subnotebooks and palmtop computers, battery-powered equipment, hand-held equipment, peripherals, and printers.

Table 1: Device summary

Order code	Temp. range	Package	Packaging
ST3232CDR	0 to 70 °C	SO16 (tape and reel)	2500 parts per reel
ST3232BDR	-40 to 85 °C		
ST3232CWR	0 to 70 °C	SO16L (tape and reel)	1000 parts per reel
ST3232BWR	-40 to 85 °C		
ST3232CTR	0 to 70 °C	TSSOP16 (tape and reel)	2500 parts per reel
ST3232BTR	-40 to 85 °C		

4.2 Construction note

	P/N ST8034TDT	**P/N TSM102/A**	**P/N ST 3232B**
Wafer/Die fab. information			
Wafer fab manufacturing location	ST Catania	ST Singapore	ST Singapore
Technology	BCD6S	Bipolar	BCD3S
Die finishing back side	RAW SILICON	RAW SILICON	Lapped SILICON
Die size (microns)	1608x1700 µm	1860x3400µm	1820x2380µm²
Bond pad metallization layers	AlCu	AlSiCu	AlSiCu
Passivation type	TEOS/SiN/Polyimide	SiN	USG-PSG-SiON-PIX
Assembly information			
Assembly site	ST Shenzhen		
Package description	SO16		
Molding compound	Sumitomo G630AY		
Frame material	Copper		
Die attach process	Glue		
Die attach material	Ablestick 8601 –S25		
Wire bonding process	Tehrmosonic ball bonding		
Wires bonding materials/diameters	Cu 1 mil		
Lead finishing process	Preplated		
Lead finishing/bump solder material	NiPdAu		

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	BCD6S / SO16	UI87	ST8034 (lot GK7510KX01)
2	Bipolar /SO16	0102	TSM102/A (lot GK8022FH01)
3	BCD3S/SO16	UW55	ST3232B (lot GK7460VM01)

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS						Note
						Lot1 UI87	Lot 2	Lot 3				
Die oriented tests												
HTB/ HTOL	N	JESD22 A-108	Ta = 125°C, BIAS		168 H							
					500 H							
					1000 H							
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/100	0/80	0/77				
					500 H	0/100	0/80	0/77				
					1000 H	On going	On going	0/77				
Package Oriented Tests												
PC		JESD22 A-113	Drying 24 H @ 125°C JL1 (Store 168 H @ Ta=85°C Rh=85%) JL2 (Store 192 H @ Ta=30°C Rh=60%) Over Reflow @ Tpeak=260°C 3 times		Final	PASS MSLS3	MSL3					
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/80	0/80	0/77				
					168h							
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		200 cy	0/80	0/80	0/77				
					500 cy	0/80	On going	0/77				
					1000cy							
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H							
					500 H							
					1000 H							

Scanning acoustic microscopy, check for delamination at die/resin interface, Lead/Resin interface and in through scan:
UI87

Device	Lot	Trial	SAM result			
			Qty	Die	Lead	T-scan
SKQ7*UI87CE5	GK7510KX01	T0	20	0/20	0/20	0/20
		MSL3	20	0/20	0/20	0/20
		TC200	20	0/20	0/20	0/20
		TC500	20	0/20	0/20	0/20
		PPT	20	0/20	0/20	0/20

UW55

Device	Lot	Trial	SAM result			
			Qty	Die	Lead	T-scan
7TI8*A6C127C	GK7460VM01	T0	20	0/20	0/20	0/20
		MSL3	20	0/20	0/20	0/20
		TC200	20	0/20	0/20	0/20
		TC500	20	0/20	0/20	0/20
		PPT	20	0/20	0/20	0/20

5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.