PCN
Product/Process Change Notification

Qualification of SMA & SMB packages at Assembly/Test location in China

Notification number:	ADG-DFD/20/12338	**Issue Date**	15/09/20
Issued by	Aline Augis		
Product series affected by the change		- Power Schottky, Ultrafast - SM6T, SMAJ and SMBJ products with • 40V <= Vrm <= 70V • 46V <= Vbr <= 82V	
Type of change		Back End Realization	

Description of the change

STMicroelectronics is qualifying a new assembly line of SMA & SMB package subcontracted in China

Reason for change

STMicroelectronics has decided to expand the manufacturing capacity of Rectifiers and TVS protection devices housed in SMA & SMB package. This additional assembly line is located in China in a subcontractor already qualified and delivering in high volume for ST.

Former versus changed product:	The changed products will remain fully compliant with product datasheet in term of electrical, dimensional or thermal parameters. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Disposition of former products

Purpose is to implement additional production capacity, shipments will be done from all qualified assembly lines.

Marking and traceability

No marking change.

Assembly location	Plant and date code		
	Assy plant code	Assy year	Assy week
China (subco current line)	GP	**Y** (1 digit indicating the year)	**WW** (2 digits indicating the week number)
China (subco new line)	**GP**		

Traceability for the implemented change will be ensured by an **internal codification (finish good)** and by the **Q.A. number**.

Qualification complete date	2020 week 34

Forecasted sample availability

All qualification samples are available on request.

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
All	**W48-2020**	**W50-2020**

Comments:	With early PCN acceptance, possible shipment starting week 41 on selected part numbers.

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	20029QRP, 20053QRP, 20047QRP

Reliability Evaluation Report

SMAJxx (VRM from 40V to 188V)
SMA6Jxx (VRM from 5V to 85V) product qualification

General Information	
Product Description	*Protection*
Finish Good(s)	*SMAJ40A-TR/CA-TR* *SMAJ43A-TR/CA-TR* *SMAJ48A-TR/CA-TR* *SMAJ58A-TR/CA-TR* *SMAJ70A-TR/CA-TR* *SMAJ85CA-TR* *SMAJ130CA-TR* *SMAJ154A-TR* *SMAJ170A-TR/CA-TR* *SMAJ188A-TR/CA-TR* *SMA6J5.0A-TR/CA-TR* *SMA6J6.0A-TR/CA-TR* *SMA6J6.5A-TR/CA-TR* *SMA6J8.5A-TR/CA-TR* *SMA6J10A-TR/CA-TR* *SMA6J12A-TR/CA-TR* *SMA6J13A-TR/CA-TR* *SMA6J15A-TR/CA-TR* *SMA6J18A-TR/CA-TR* *SMA6J20A-TR/CA-TR* *SMA6J24A-TR/CA-TR* *SMA6J26A-TR/CA-TR* *SMA6J28A-TR/CA-TR* *SMA6J33A-TR/CA-TR* *SMA6J40A-TR/CA-TR* *SMA6J48A-TR/CA-TR* *SMA6J58A-TR/CA-TR* *SMA6J70A-TR/CA-TR* *SMA6J85A-TR/CA-TR*
Product Group	*ADG*
Product division	*DFD*
Package	*SMA*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST TOURS FRANCE*
Assembly plant	*SUBCONTRACTOR IN CHINA* *9941*
Reliability Lab	*ST TOURS FRANCE*

Reliability Assessment
PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1	28/05/2020	8	Aude DROMEL	Julien MICHELON	Initial release
2	12/08/2020	13	Julien MICHELON	Julien MICHELON	Adding products

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
ADG-DIS/20/12045	Industrial grade qualification of TVS in SMA and SMB packages at Assembly/Test location in China

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
PC	Pre-conditioning
THB / H3TRB	Thermal Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test
DPA	Destructive Physical Analysis
RSH	Resistance to Solder Heat
SD	Solderability
MSL	Moisture Sensitivity Level
DBT	Dead Bug Test
GD	Generic data

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective is to qualify SMA package at our subcontractor in China for SMA6J protection devices from 5V to 85V (VRM) & SMAJ protection devices from 40V to 188V (VRM).

3.2 Conclusion

Qualification plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

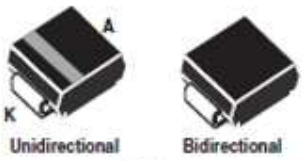
4.1 Device description

life.augmented

SMA6J

High junction temperature Transil™

Datasheet - production data



SMA
(JEDEC DO-214AC)

Features

- Peak pulse power:
  - 600 W (10/1000 µs)
  - 4 kW (8/20 µs)
- Stand off voltage range: from 5 V to 188 V
- Unidirectional and bidirectional types
- Low clamping voltage versus standard series
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating T_j max: 175 °C
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G-Method 3015-7: class3B
  - 25 kV (human body model)

Description

The SMA6J Transil series has been designed to protect sensitive equipment against electro-static discharges according to IEC 61000-4-2, MIL STD 883 Method 3015, and electrical over stress such as IEC 61000-4-4 and 5. They are generally for surges below 600 W 10/1000 µs.

This planar technology makes it compatible with high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time. Their low clamping voltages provides a better safety margin to protect sensitive circuits with extended life time expectancy.

Packaged in SMA, this minimizes PCB space consumption (SMA footprint in accordance with IPC 7531 standard).

SMAJ

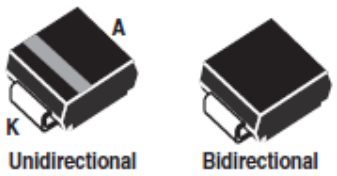
Transil™

Features

- Peak pulse power:
  - 400 W (10/1000 µs)
  - 2.3 kW (8/20 µs)
- Stand off voltage range: from 5 V to 188 V
- Unidirectional and bidirectional types
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating $T_{j\,max}$: 150 °C
- High power capability at $T_{j\,max}$:
  - 270 W (10/1000 µs)
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-5 (see Table 3 for surge level)
- MIL STD 883G, method 3015-7 Class 3B
  - 25 kV HBM (human body model)
- Resin meets UL 94, V0
- MIL-STD-750, method 2026 solderability
- EIA STD RS-481 and IEC 60286-3 packing
- IPC 7531 footprint



Unidirectional Bidirectional

SMA
(JEDEC DO-214AC)

Description

The SMAJ Transil series has been designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2, and MIL STD 883, method 3015, and electrical over stress according to IEC 61000-4-4 and 5. These devices are generally used against surges below 400 W (10/1000 µs).

Planar technology makes these devices suitable for high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

SMAJ are packaged in SMA (SMA footprint in accordance with IPC 7531 standard).

4.2 Construction note

	SMA6JxxA-TR / CA-TR (xx VRM from 5V to 85V)
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS GLOBAL 6"
Technology / Process family	DISCRETE-TRANSIL / TAN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR IN CHINA
Package description	SMA
Final testing information	
Testing location	SUBCONTRACTOR IN CHINA

	SMAJxxA-TR / CA-TR (xx VRM from 40V to 188V)
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS GLOBAL 6"
Technology / Process family	DISCRETE-TRANSIL / TAN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR IN CHINA
Package description	SMA
Final testing information	
Testing location	SUBCONTRACTOR IN CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Die manufacturing plant	Assembly plant	Package	Comments
Lot 1	SMA6J5.0A-TR	ST TOURS	SUBCONTRACTOR CHINA	SMA	Qualification lots
Lot 2	SMA6J33A-TR				
Lot 3	SMA6J33CA-TR				
Lot 4	SMAJ188CA				
Lot 5	SMA6J85A				
Lot 6	SMA6J85CA				
Lot 7	SM4T82AY				
Lot 8	SM4T82CAY				
Lot 9	SMA6T82AY				
GD1	SMA6T39CAY				Similar package for solderability trials
GD2	Dummy SMD	NA	NA		Similar package for whiskers

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.		
						Lot 1 5V UNI IPP 11.8A	**Lot 2** 33V UNI IPP 68A	**Lot 3** 33V BI IPP 68A
Die Oriented Tests								
Repetitive Surge	Y	ADCS0060282	IPP (10/1000us)=max datasheet value	60	50 surges	0/20	0/20	0/20
					1000 surges	0/20	0/20	0/20
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=175°C Voltage=VRM	231	504h	0/77	0/77	0/77
					1000h	0/77	0/77	0/77
Package Oriented Tests								
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-55°C	77	500cy	-	0/77	-
					1000cy	-	0/77	-
H3TRB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=VRM	77	168h	-	0/77	-
					504h	-	0/77	-
					1000h	-	0/77	-
UHAST	Y	JESD22 A-118	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	77	96h	-	-	0/77

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.					
						Lot 4 188V Bi 400W	**Lot 5** 85V Uni 600W	**Lot 6** 85V Bi 600W	**Lot 7** 70V Uni 400W	**Lot 8** 70V Bi 400W	**Lot 9** 70V Uni 600W
Die Oriented Tests											
Repetitive Surge	N	ADCS0060282	IPP (10/1000us)=max datasheet value	100	measure at 50s	0/20	0/20	0/20	0/20	-	0/20
					measure at 1000s	0/20	0/20	0/20	0/20	-	0/20
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=175°C Temperature=175°C Tension=VRM	154	504h	0/77	-	-	-	-	0/77
					1000h	0/77	-	-	-	-	0/77
Package Oriented Tests											
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	231	500cy	-	0/77	0/77	0/77	-	-
					1000cy	-	0/77	0/77	0/77	-	-
RSH	N	JESD22A-111 (SMD) / JESD22B-106 (PTH)	Temperature=260°C Time (on)=10s	30	dipping	-	-	-	-	-	0/30
H3TRB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=VRM	154	168h	-	-	0/77	-	0/77	-
					504h	-	-	0/77	-	0/77	-
					1000h	-	-	0/77	-	0/77	-
UHAST	Y	JESD22 A-118	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	154	96h	-	-	0/77	-	-	0/77
MSL search	Y	JESD22-A113	Humidity (HR)=85% Temperature=85°C MSL=1 Reflow=3	30	168h	-	-	-	-	-	0/30

For solderability oriented trials similarities are done with the SMA6T39CAY (SMA package).

Test	PC	Std ref.	Conditions	SS	Steps	Failure /SS	
						GD1 33V Bi auto	GD2
Solderability	N	J-STD-002	Steam Ageing SnAgCu bath 245°C	60	Visual inspection	0/15	-
			Steam Ageing SnPb 220°C			0/15	-
			Dry Ageing SnAgCu 245°C			0/15	-
			Dry Ageing SnPb 220°C			0/15	-
DBT	N	DM 00112629	Fluxing followed by IR reflow.	30	Visual inspection	0/30 Compliant	-
Whiskers	Y	AEC-Q005 JESD201	Pb free reflow TC -55°C/85°C 3 cycles/hrs	18	1500cy	-	0/18
			Pb free reflow THS 30°C/RH = 60%	18	4000hrs	-	0/18
			Pb free reflow THS 55°C / RH = 85%	18	4000hrs	-	0/18
			No reflow TC -55°C/85°C 10 min	18	1500cy	-	0/18
			No reflow THS 30°C / RH = 60%	18	4000hrs	-	0/18
			No reflow THS 55°C / RH = 85%	18	4000hrs	-	0/18
			SnPb reflow TC -55°C/85°C 10 min	18	1500cy	-	0/18
			SnPb reflow THS 30°C / RH = 60%	18	4000hrs	-	0/18
			SnPb reflow THS 55°C / RH = 85%	18	4000hrs	-	0/18

6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Repetitive surges	ADCS0060282	Devices are submitted to rated Ipp for 1000 surges.	Purpose: This test is intended to verify robustness of device submitted to rated Ipp (as per data sheet) = exploration of reverse characteristic at a calibrated current value followed by the measure of voltage clamping value. Failure mode expected is short circuit of the device due to hot spot creation into silicon bulk at device periphery where the electrical field gradient is the most important. Physical analysis must be done to verify consistency of the failure mode and discriminate from extrinsic causes related to process escapes.
Package Oriented			
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Standard Reference	Description	Purpose
PC Preconditioning	JESD22 A-113	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
THB/H3TRB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
uHAST	JESD22 A-118	The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments .	Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DPA Destructive Physical Analysis	AEC Q101-004	Specific construction analysis on random parts that have successfully completed THB or TC.	To investigate on reliability stresses impact on delamination, corrosion and product construction integrity.
Whiskers	AEC-Q005 JESD201	This test is intended to check Tin plated packages quality versus whiskers risk.	It is applicable for studying tin whisker growth from finishes containing a predominance of tin (Sn).
RSH Resistance to solder heat	ST 0060102 JESD22 B-106-A	Device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.

Test name	Standard Reference	Description	Purpose
DBT	DM00112629	To evaluate the wettability of the SMD. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.

Reliability Evaluation Report

Qualification of Power Schottky & Bipolar Rectifiers in SMA & SMB packages at existing Assembly/Test location in China

General Information	
Product Line	*Rectifiers*
Product Description	*Power Schottky & Bipolar rectifiers*
Product perimeter	*STPS1H100A, STPS2H100A, STPS1L60A, STPS1L40A, STPS130A, STPS140A, STPS1150A, STPS160A, STPS1L30A, STPS2L30A, STPS2L60A, STPS2150A, STTH102A, STTH1R02A, STTH1R04A, STTH2R02A* *STPS1H100U, STPS1L40U, STPS130U, STPS140U, STPS2H100U, STPS3H100U, STPS160U, STPS1L30U, STPS2L25U, STPS340U, STPS3L60U, STPS3150U, STPS2L40U, STPS2200U, STTH1R02U, STTH1R04U, STTH2R02U, STTH4R02U, STTH504U, STTH3R04U*
Product Group	*ADG*
Product division	*Discrete & Filter*
Package	*SMA / SMB*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST SINGAPORE* *ST TOURS*
Assembly plant	*ST Subcontractor* *9941 - CHINA*
Reliability Lab	*ST TOURS - FRANCE*
Reliability assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	14-Sept-2020	12	Christophe GOIN	Julien MICHELON	Initial release

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices
AEC-Q005	Pb-Free Test Requirements

2 GLOSSARY

SS	Sample Size
PC	Pre-Conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
H3TRB	High Humidity High Temperature Reverse Bias
IOLT	Intermittent Operating Life Test
UHAST	Unbiased Highly Accelerated Stress Test
DPA	Destructive Physical Analysis (after TC and THB)
GD	Generic Data
SD	Solderability test
RSH	Resistance to Soldering Heat
THS	Temperature Humidity Storage

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify additional assembly line for rectifiers housed in SMA and SMB packages in a subcontractor located in China, already qualified and delivering in high volume for ST.

The involved products are listed in the table here below:

Product	Product Family	Package	Assembly Location
STPS1H100A	POWER SCHOTTKY	SMA	Subcontractor – CHINA (9941)
STPS1L60A			
STPS1L40A			
STPS130A			
STPS140A			
STPS1150A			
STPS2H100A			
STPS160A			
STPS1L30A			
STPS2L30A			
STPS2L60A			
STPS2150A			
STTH102A	BIPOLAR RECTIFIER		
STTH1R02A			
STTH1R04A			
STTH2R02A			
STPS1H100U	POWER SCHOTTKY	SMB	
STPS1L40U			
STPS130U			
STPS140U			
STPS2H100U			
STPS3H100U			
STPS160U			
STPS1L30U			
STPS2L25U			
STPS340U			
STPS3L60U			
STPS3150U			
STPS2L40U			
STPS2200U			
STTH1R02U	BIPOLAR RECTIFIER		
STTH1R04U			
STTH2R02U			
STTH4R02U			
STTH504U			
STTH3R04U			

Change description:

The changed products will remain fully compliant with product datasheet in term of electrical, dimensional or thermal parameters.

The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged.

The footprint recommended by ST remains the same.

There is no change in the packing modes and the standard delivery quantities either.

The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Reliability tests description:

The reliability test methodology used follows the JESD47: « Stress Test riven Qualification Methodology ».

The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH and Solderability to check compatibility of package with customer assembly.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Example of ST specification:

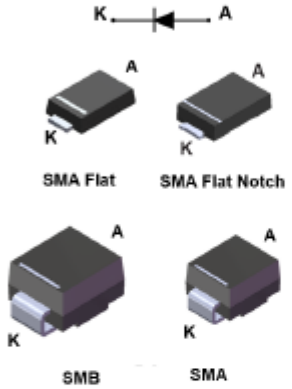
Power Schottky product:

life.augmented

STPS1H100

Datasheet

100 V, 1 A power Schottky rectifier



Features

- Negligible switching losses
- High junction temperature capability
- Low leakage current
- Good trade off between leakage current and forward voltage drop
- Avalanche capability specified
- ECOPACK2 halogen-free component

Description

Schottky rectifiers designed for high frequency miniature switched mode power supplies such as adaptors and on board DC/DC converters.

Packaged in SMA, SMA Flat, SMA Flat Notch,or SMB, this diode is ideal for use in lighting and telecom power applications.

Product status
STPS1H100

Product summary	
Symbol	**Value**
$I_{F(AV)}$	1 A
V_{RRM}	100 V
$T_{j(max.)}$	175 °C
$V_{F(max.)}$	0.62 V

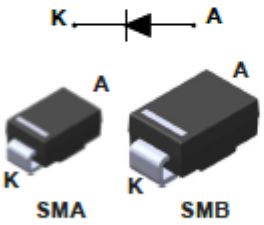
Bipolar product:

life.augmented

STTH1R04

Datasheet

1 A - 400 V ultrafast recovery diode



SMA SMB

DO-15

Features

- Negligible switching losses
- Low forward voltage drop
- High junction temperature
- ECOPACK compliant

Applications

- Switching diode
- Telecom power

Description

The STTH1R04 series uses ST's new 400 V planar Pt doping technology. The STTH1R04 is specially suited for switching mode base drive and transistor circuits.

Packaged in SMA, SMB and DO-15, the STTH1R04 is ideal for use low voltage, high frequency inverters, free wheeling and polarity protection

Product status
STTH1R04

Product summary	
Symbol	**Value**
$I_{F(AV)}$	1 A
V_{RRM}	400 V
$T_{j(max.)}$	175 °C
$V_{F(typ.)}$	0.9 V
trr(typ.)	14 ns

4.2 Construction Note

	Power Schottky Products
Wafer/Die fab. information	
Wafer fab manufacturing location	ST SINGAPORE
Technology / Process family	Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	Subcontractor – CHINA
Package description	SMA CLIP / SMB CLIP
Final testing information	
Testing location	Subcontractor – CHINA

	Bipolar Products
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours
Technology / Process family	Bipolar Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours
Assembly information	
Assembly site	Subcontractor – CHINA
Package description	SMA CLIP / SMB CLIP
Final testing information	
Testing location	Subcontractor – CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	STPS5L60U	SMB	Qualification lot 1 (largest die)
L2	STPS3150UY	SMB	Qualification lot 2 (highest voltage for Power Schottky)
L3	STTH1R04	SMA	Qualification lot 3 (highest voltage for Bipolar)
GD1	Generic data	SMA	Generic data for thermomechanical and hermeticity related tests
GD2	Generic data	SMB	Generic data for thermomechanical and hermeticity related tests
GD3	Generic data	SMB	Generic data for thermomechanical and hermeticity related tests
GD4	Generic data	SMA	Generic data for solderability on SMA package
GD5	Generic data	SMB	Generic data for solderability on SMB package
GD6	Generic data	SMA & SMB	Generic data for Tin whiskers on SMA & SMB packages

Detailed results in below chapter will refer to these references.

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.								
						Lot 1	Lot 2	Lot 3	GD 1	GD 2	GD 3	GD 4	GD 5	GD6
Die Oriented Tests														
Pre and Post Electrical Test			I_R, V_F parameters following product datasheet	231	-	0/231								
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=75°C Voltage=48V	77	1000h	0/77								
			Junction Temperature=130°C Voltage=150V	77	1000h		0/77							
			Junction Temperature=175°C Voltage=400V	77	1000h			0/77						
Package Oriented Tests														
Pre and Post Electrical Test			I_R, V_F parameters following product datasheet	1138	-	0/1138								
TC	N	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	77	500cy	0/77		0/77		0/77	0/77			
H3TRB	N	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=100V	154	1000h			0/77			0/77			
			Humidity (HR)=93% Temperature=60°C Voltage=48V	77	1000h	0/77								
UHAST	N	JESD22 A-118	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	231	96h		0/77	0/77			0/77			
IOLT	N	MIL-STD 750 Method 1037	Delta Tj=125°C Intensity (If)=3.15A Time (off)=120s Time (on)=120s	77	500h	0/77								
			Delta Tj=100°C Intensity (If)=0.8A Time (off)=120s Time (on)=120s	154	1000h			0/77		0/77				
			Delta Tj=100°C Intensity (If)=1A Time (off)=120s Time (on)=120s	77	1000h						0/77			
RSH	N	JESD22A-111	Temperature=260°C Time (on)=10s	60	-	0/30			0/30					
SD	Y	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	30	-							0/15	0/15	
			Dry ageing SnPb bath 220°C	30	-							0/15	0/15	
			Wet ageing SnAgCu bath 245°C	30	-							0/15	0/15	
			Dry ageing SnAgCu bath 245°C	30	-							0/15	0/15	

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.								
						Lot 1	Lot 2	Lot 3	GD 1	GD 2	GD 3	GD 4	GD 5	GD6
Whiskers	Y	AEC-Q005 JESD201	Pb free reflow TC -55°C / +85°C	18	1500cy									0/18
			Pb free reflow THS 30°C / RH = 60%	18	4000h									0/18
			Pb free reflow THS 55°C / RH = 85%	18	4000h									0/18
			No reflow TC -55°C / +85°C	18	1500cy									0/18
			No reflow THS 30°C / RH = 60%	18	4000h									0/18
			No reflow THS 55°C / RH = 85%	18	4000h									0/18
			SnPb reflow TC -55°C / +85°C	18	1500cy									0/18
			SnPb reflow THS 30°C / RH = 60%	18	4000h									0/18
			SnPb reflow THS 55°C / RH = 85%	18	4000h									0/18

6 ANNEXES

6.1 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse	The diode is biased in static reverse mode at targeted junction temperature.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature.	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
RSH Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
SD Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
Whiskers	Forced growing of Tin Whiskers by various kind of environmental stress: temperature, moisture and temperature cycling.	To ensure no risk of electrical short due to Tin Whisker growth.

Reliability Evaluation Report

SMBJxx (VRM from 36V to 85V)
SM6Txx (VBR from 56V to 100V) product qualification

General Information	
Product Description	*Protection* *SMBJ36CA-TR* *SMBJ40A-TR/CA-TR* *SMBJ48A-TR/CA-TR* *SMBJ58A-TR/CA-TR* *SMBJ64A-TR/CA-TR* *SMBJ70A-TR/CA-TR* *SMBJ85CA-TR*
Finish Good(s)	*SM6T56CA* *SM6T68A/CA*
Product Group	*ADG*
Product division	*DFD*
Package	*SMB*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST TOURS FRANCE*
Assembly plant	*SUBCONTRACTOR IN CHINA* *9941*
Reliability Lab	*ST TOURS FRANCE*

Reliability Assessment
PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1	12/08/2020	13	Julien MICHELON	Julien MICHELON	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
ADG-DIS/20/12045	Industrial grade qualification of TVS in SMA and SMB packages at Assembly/Test location in China

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
PC	Pre-conditioning
THB / H3TRB	Thermal Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test
DPA	Destructive Physical Analysis
RSH	Resistance to Solder Heat
SD	Solderability
MSL	Moisture Sensitivity Level
DBT	Dead Bug Test
GD	Generic data

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective is to qualify SMB package at our subcontractor in China for SMBJ protection devices from 36V to 85V (VRM) & SM6T protection devices from 56V to 100V (VBR).

3.2 Conclusion

Qualification plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

SMBJ

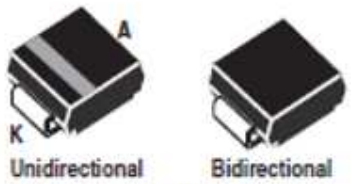
Transil™

Features

- Peak pulse power:
  - 600 W (10/1000 µs)
  - 4 kW (8/20 µs)
- Stand off voltage range: from 5 V to 188 V
- Unidirectional and bidirectional types
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating $T_{j\,max}$: 150 °C
- High power capability at $T_{j\,max}$:
  - 515 W (10/1000 µs)
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-5
- MIL STD 883G, method 3015-7 Class 3B:
  - 25 kV HBM (human body model)
- Resin meets UL 94, V0
- MIL-STD-750, method 2026 soldererability
- EIA STD RS-481 and IEC 60286-3 packing
- IPC 7531 footprint



SMB
(JEDEC DO-214AA)

Description

The SMBJ Transil series has been designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2, and MIL STD 883, method 3015, and electrical over stress according to IEC 61000-4-4 and 5. These devices are more generally used against surges below 600 W (10/1000 µs).

Planar technology makes these devices suitable for high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

SMBJ are packaged in SMB (SMB footprint in accordance with IPC 7531 standard).

SM6T

Transil™

Features

- Peak pulse power:
  - 600 W (10/1000 µs)
  - 4 kW (8/20 µs)
- Breakdown voltage range: from 6.8 V to 220 V
- Unidirectional and bidirectional types
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating $T_{j\,max}$: 150 °C
- High power capability at T_{jmax}:
  - 515 W (10/1000 µs)
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-5
- MIL STD 883G, method 3015-7: class 3B:
  - 25 kV HBM (human body model)
- UL 497B, file number: QVGQ2.E136224
- Resin meets UL 94, V0
- MIL-STD-750, method 2026 solderability
- EIA STD RS-481 and IEC 60286-3 packing
- IPC 7531 footprint

Unidirectional Bidirectional

SMB
(JEDEC DO-214AA)

Description

The SM6T Transil series has been designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2 and MIL STD 883, method 3015, and electrical overstress according to IEC 61000-4-4 and 5. These devices are more generally used against surges below 600 W (10/1000 µs).

Planar technology makes these devices suitable for high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

SM6T are packaged in SMB (SMB footprint in accordance with IPC 7531 standard).

TM: Transil is a trademark of STMicroelectronics

4.2 Construction note

	SMBJxxA-TR / CA-TR (xx VRM from 36V to 85V)
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS GLOBAL 6"
Technology / Process family	DISCRETE-TRANSIL / TAN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR IN CHINA
Package description	SMB
Final testing information	
Testing location	SUBCONTRACTOR IN CHINA

	SM6TxxA-TR / CA-TR (xx VBR from 56V to 100V)
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS GLOBAL 6"
Technology / Process family	DISCRETE-TRANSIL / TAN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR IN CHINA
Package description	SMB
Final testing information	
Testing location	SUBCONTRACTOR IN CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Die manufacturing plant	Assembly plant	Package	Comments
Lot 1	SMBJ70A-TR	ST TOURS	SUBCONTRACTOR CHINA	SMB	Qualification lots
Lot 2	SM6T82CAY				
Lot 3	SMBJ64A-TR				
Lot 4	SM6T100A				
GD1	SM6T39CAY				Same package, same die size, same BOM
GD2	SM6T6V8CA				
GD3	SM6T36A				
GD4	Dummy SMD	NA	NA	SMD	Similar package for whiskers

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.			
						Lot 1 SMBJ70A	**Lot 2** SM6T82CA	**Lot 3** SMBJ64A	**Lot 4** SM6T100A
Repetitive Surge	Y	ADCS0060282	IPP(10/1000us)=Max datasheet value	60	measure at 50s	-	0/20	0/20	0/20
					measure at 1000s	-	0/20	0/20	0/20
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=150°C Voltage=VRM	231	168h	-	0/77	0/77	0/77
					1000h	-	0/77	0/77	0/77
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	231	500cy	0/77	-	0/77	0/77
					1000cy	0/77	-	0/77	0/77
H3TRB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=VRM	231	168h	-	-	0/77	0/77
					1000h	-	0/77	0/77	0/77

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		
						GD1 SM6T39CAY	**GD2** SM6T6V8CA	**GD3** SM6T36A
Package Oriented Tests								
uHAST	Y	JESD22-A110-B	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	231	96h	0/77	0/77	0/77
MSL search	N	JESD22 A-113	Humidity (HR)=85% Temperature=85°C MSL=1 Reflow=3	30	168h	0/30	-	-
RSH	Y	ST 0060102 JESD22 A-111	Temperature=260°C Time (on)=10s	30	dipping	0/30	-	-
DBT	N	DM 00112629	Fluxing followed by IR reflow.	30	Visual Inspection	0/30	-	-
Solderability	N	JESD22 B-102	Steam Ageing SnAgCu bath	10	Visual	0/10	-	-
			Steam Ageing SnPb bath	10	Visual	0/10	-	-
			Dry Ageing SnAgCu bath	10	Visual	0/10	-	-
			Dry Ageing SnPb bath	10	Visual	0/10	-	-

Test	PC	Std ref.	Conditions	SS	Steps	Failure /SS GD4 Dummy SMD
Package Oriented Tests						
Whiskers	Y	AEC-Q005 JESD201	Pb free reflow TC -55°C/85°C	18	1500cy	0/18
			Pb free reflow THS 30°C/RH = 60%	18	4000hrs	0/18
			Pb free reflow THS 55°C / RH = 85%	18	4000hrs	0/18
			No reflow TC -55°C/85°C 10 min	18	1500cy	0/18
			No reflow THS 30°C / RH = 60%	18	4000hrs	0/18
			No reflow THS 55°C / RH = 85%	18	4000hrs	0/18
			SnPb reflow TC -55°C/85°C 10 min	18	1500cy	0/18
			SnPb reflow THS 30°C / RH = 60%	18	4000hrs	0/18
			SnPb reflow THS 55°C / RH = 85%	18	4000hrs	0/18

6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Repetitive surges	ADCS0060282	Devices are submitted to rated Ipp for 1000 surges.	Purpose: This test is intended to verify robustness of device submitted to rated Ipp (as per data sheet) = exploration of reverse characteristic at a calibrated current value followed by the measure of voltage clamping value. Failure mode expected is short circuit of the device due to hot spot creation into silicon bulk at device periphery where the electrical field gradient is the most important. Physical analysis must be done to verify consistency of the failure mode and discriminate from extrinsic causes related to process escapes.
Package Oriented			
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Standard Reference	Description	Purpose
PC Preconditioning	JESD22 A-113	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
THB/H3TRB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
uHAST	JESD22 A-118	The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments .	Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DPA Destructive Physical Analysis	AEC Q101-004	Specific construction analysis on random parts that have successfully completed THB or TC.	To investigate on reliability stresses impact on delamination, corrosion and product construction integrity.
Whiskers	AEC-Q005 JESD201	This test is intended to check Tin plated packages quality versus whiskers risk.	It is applicable for studying tin whisker growth from finishes containing a predominance of tin (Sn).
RSH Resistance to solder heat	ST 0060102 JESD22 B-106-A	Device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.

Test name	Standard Reference	Description	Purpose
DBT	DM00112629	To evaluate the wettability of the SMD. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.