



**MICROCHIP**

# **QUALIFICATION PLAN**

**PCN #: JAON-01QMAQ209**

**Date:  
Mar 25, 2015**

**Qualification of LPI assembly site as an additional site for  
selected products in 8L SOIC package.**

Distribution

Surasit P.  
Wanphen L.  
Wichai K.  
Fernando C.  
Chalermpon P.

Rangsun K.  
A. Navarro  
Chaweng W.  
Oliver B.

Microchip Technology (Thailand) Co., Ltd.  
14 Moo 1 T. Wangtakien A. Muangchacherngsao,  
Chacherngsao, Thailand, 24000  
Tel. (6638) 857119-45, 857311-19 ext. 1231  
Fax (6638) 857149-50

**Purpose:** \_\_\_\_\_ Qualification of LPI assembly site as an additional site  
for selected products in 8L SOIC package.

**MP code:** \_\_\_\_\_ DEDX2

**Part No.:** \_\_\_\_\_ 24LC512

**BD No.:** \_\_\_\_\_ BDM-000731 rev.A

**CCB No.:** \_\_\_\_\_ 1566.01

**Package:**

**Type** \_\_\_\_\_ 8L SOIC

**Width or Size** \_\_\_\_\_ 150 mils

**Die thickness:** \_\_\_\_\_ 15 mils

**Die size:** \_\_\_\_\_ 78.7 x 111.0 mils

**Lead frame:**

**Paddle size:** \_\_\_\_\_ 95 x 130 mils

**Material** \_\_\_\_\_ CDA194

**Surface** \_\_\_\_\_ Ag spot

**Process** \_\_\_\_\_ Stamp

**Lead Lock** \_\_\_\_\_ No

**Part Number** \_\_\_\_\_ 09S000823

**Treatment** \_\_\_\_\_ None

**Wire:**

**Material** \_\_\_\_\_ Au

**Die Attach Epoxy:**

**Part Number** \_\_\_\_\_ 8340

**Conductive** \_\_\_\_\_ Yes

**Mold Compound:** \_\_\_\_\_ G600

**Lead finish** \_\_\_\_\_ Matte tin

| Test Name                      | Conditions   | Sample Size   | Min. Qty of Spares per Lot (should be properly marked) | Qty of Lots | Total Units | Fail Accept Qty     | Est. Dur. Days | Special Instructions  |
|--------------------------------|--|---|--|-------------|-------------|---------------------|----------------|---|
| Standard Pb-free Solderability | JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing.<br><br>Standard Pb-free: Matte tin/ NiPdAu finish, SAC solder, wetting temp 245°C for both SMD & through hole packages. | 22  | 5  | 1           | 27          | > 95% lead coverage | 5              | Standard Pb-free solderability is the requirement. SnPb solderability (backward solderability—SMD reflow soldering) is required for any plating related changes and highly recommended for other package BOM changes. |
| Standard SnPb Solderability    | JESD22B-102E; Perform 8 hour steam aging prior to testing.<br><br>Standard SnPb: SnPb finish, SnPb solder, wetting temp 215°C for SMD & 245°C for through hole packages.   | 22  | 5  | 1           | 27          | > 95% lead coverage | 5              |   |
| Backward Solderability         | JESD22B-102E; Perform 8 hours steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing.<br><br>Backward: Matte tin/ NiPdAu finish, SnPb solder, wetting temp 215°C for SMD.                                    | 22  | 5  | 1           | 27          | > 95% lead coverage | 5              |   |
| Wire Bond Pull - WBP           | Mil. Std. 883-2011   | 5   | 0  | 1           | 5           | 0 fails after TC    | 5              | 30 bonds from a minimum of 5 devices.   |
| Wire Bond Shear - WBS          | CDF-AEC-Q100-001   | 5   | 0  | 1           | 5           | 0                   | 5              | 30 bonds from a minimum of 5 devices.   |
| Physical Dimensions            | Measure per JESD22 B100 and B108   | 10  | 0  | 3           | 30          | 0                   | 5              |   |
| External Visual                | Mil. Std. 883-2009/2010  | All devices prior to submission for qualification testing | 0  | 3           | ALL         | 0                   | 5              |   |
| HTSL (High Temp Storage Life)  | +175 C for 504 hours or 150°C for 1008 hrs. Electrical test pre and post stress at +25C and hot temp.  | 45  | 5  | 1           | 50          | 0                   | 10             | Must be in progress at time of package release to production, but completion is not required for release to production.   |

| Test Name  | Conditions   | Sample Size | Min. Qty of Spares per Lot (should be properly marked) | Qty of Lots | Total Units | Fail Accept Qty | Est. Dur. Days | Special Instructions  |
|--|--|-------------|--|-------------|-------------|-----------------|----------------|---|
| Preconditioning - Required for surface mount devices | +150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020D for package type; Electrical test pre and post stress at +25°C.<br>MSL-1 @ 260°C | 231         | 15   | 4           | 984         | 0               | 15             | Spares should be properly identified. 77 parts from each lot to be used for HAST, Autoclave, Temp Cycle test. |
| HAST   | +130°C/85% RH for 96 hours. Electrical test pre and post stress at +25°C and hot temp.<br>1 lot tested at 125C   | 77          | 5  | 4           | 328         | 0               | 10             | Spares should be properly identified. Use the parts which have gone through Pre-conditioning.                 |
| Unbiased HAST  | +130°C/85% RH for 96 hrs   | 77          | 5  | 4           | 328         | 0               | 10             | Spares should be properly identified. Use the parts which have gone through Pre-conditioning.                 |
| Temp Cycle   | -65°C to +150°C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress.<br>1 lot tested at 125C                            | 77          | 5  | 4           | 328         | 0               | 15             | Spares should be properly identified. Use the parts which have gone through Pre-conditioning.                 |