

**Assembly Relocation to Select LQFP, LQFP\_EP, MQFP, TQFP, TQFP\_EP  
Products to STATS ChipPAC China Jiangyin**

## Automotive Qualification Results Summary for LQFP at STATS ChipPAC China Jiangyin

TEST	SPECIFICATION	SAMPLE SIZE	RESULTS
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 77	PASS
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	PASS
Highly Accelerated Stress Test (HAST)*	JEDEC <i>JESD22-A110</i>	3 x 77	PASS
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 77	PASS
High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	1 x 77	PASS
Electrostatic Discharge <i>Field Induced Charge Device Model – All Pins</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±500V
Electrostatic Discharge <i>Field Induced Charge Device Model – Corner Pins</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±750V

\* These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples were subjected to wire-pull test after 500 cycles where results passed within specification limits.

**Assembly Relocation to Select LQFP, LQFP\_EP, MQFP, TQFP, TQFP\_EP  
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## Automotive Qualification Results Summary for LQFP\_EP and MQFP at STATS ChipPAC China Jiangyin

TEST	SPECIFICATION	SAMPLE SIZE	RESULTS
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 32	PASS
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	PASS
Temperature, Humidity and Bias (THB)*	JEDEC <i>JESD22-A101</i>	3 x 32	PASS
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 32	PASS
High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	1 x 32	PASS
Electrostatic Discharge <i>Field Induced Charge Device Model – All Pins</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±500V
Electrostatic Discharge <i>Field Induced Charge Device Model – Corner Pins</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±750V

\* These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples were subjected to wire-pull test after 500 cycles where results passed within specification limits.

**Assembly Relocation of Select LQFP, LQFP\_EP, MQFP, TQFP, TQFP\_EP  
Products to STATS ChipPAC China Jiangyin**

**Qualification Results Summary for  
TQFP and TQFP\_EP at STATS ChipPAC China Jiangyin**

TEST	SPECIFICATION	SAMPLE SIZE	RESULTS
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 32	PASS
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	PASS
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 32	PASS
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±1250V

\* Preconditioned per JEDEC/IPC J-STD0020.