

**Assembly Relocation of Select LQFP, LQFP_EP, MQFP, TQFP, TQFP_EP
Products to STATS ChipPAC China Jiangyin**

**Automotive Qualification Plan Summary for LQFP_EP and
MQFP at STATS ChipPAC China Jiangyin**

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 32	October 2016
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	October 2016
Temperature Humidity and Bias Test (THB)*	JEDEC <i>JESD22-A110</i>	3 x 32	October 2016
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 32	October 2016
High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	1 x 32	October 2016
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	JEDEC <i>JESD22-C101</i>	3/voltage	October 2016

* These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples will be subjected to wire-pull test after 500 cycles where results should be within specification limits.

**Assembly Relocation to Select LQFP, LQFP_EP, MQFP, TQFP, TQFP_EP
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Automotive Qualification Results Summary for LQFP at STATS ChipPAC China Jiangyin

TEST	SPECIFICATION	SAMPLE SIZE	RESULTS
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 77	PASS
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	PASS
Highly Accelerated Stress Test (HAST)*	JEDEC <i>JESD22-A110</i>	3 x 77	PASS
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 77	PASS
High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	1 x 77	PASS
Electrostatic Discharge <i>Field Induced Charge Device Model – All Pins</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±500V
Electrostatic Discharge <i>Field Induced Charge Device Model – Corner Pins</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±750V

* These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples were subjected to wire-pull test after 500 cycles where results passed within specification limits.

**Assembly Relocation of Select LQFP, LQFP_EP, MQFP, TQFP, TQFP_EP
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**Qualification Results Summary for
TQFP and TQFP_EP at STATS ChipPAC China Jiangyin**

TEST	SPECIFICATION	SAMPLE SIZE	RESULTS
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 32	PASS
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	PASS
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 32	PASS
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	JEDEC <i>JESD22-C101</i>	3/voltage	PASS ±1250V

* Preconditioned per JEDEC/IPC J-STD0020.