United Silicon Carbide, Inc.

Assembly Site Transfer Qualification Report

Discrete TO-220 SiC Diode Devices

Included Products:

TO-220-2L

UJ3D1202TS

UJ3D1205TS

UJ3D1210TS

UJ3D1210KS

UJ3D1220TS

UJ3D06504TS

UJ3D06506TS

UJ3D06508TS

UJ3D06510TS

UJ3D06512TS

UJ3D06516TS

UJ3D06520TS

UJ3D06530TS

This report summarizes the AEC-Q101 qualification results for an Assembly Site Transfer for United Silicon Carbide, Inc.'s UJ3D Discrete SiC Diodes in TO-220 plastic package.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift performance satisfies the AEC-Q101 qualification requirements, as well as UnitedSiC's Quality requirements.

Reliability Stress Test Summary

Test Name	Test Standard	# Samples x # Lots	Failures
High Temperature Reverse Bias (HTRB)	JESD22 A108 (1000 Hours) T_J=175°C, V_{DS}=960V,	77pcs x 3 lots	0/231
High Humidity High Temperature Reverse Bias (H3TRB)	JESD22 A-101D (1000 Hours) T_A=85°C/85%RH, V_{DS}=100V	77x3 lots	0/231
Intermittent Operating Life (IOL)	MIL-STD-750 Method 1037 DT_J ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)	77x3 lots	0/231
Temperature Cycle (TC)	JESD22 A-104 (1000 Cycles) -55°C to +150°C	77x3 lots	0/231
Autoclave (PCT)	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	77x3 lots	0/231
Parametric Verification	Per Datasheet	100% FT x 3 lots	
Physical Dimensions	Per AEC-Q101 Rev D	30x1 packages	0/30
Bondline Thickness	Per Assembly Spec	10x3 lots	0/30
Die Shear	Per Assembly Spec	10x3 lots	0/30
Die Attach Voids	Per Assembly Spec	10x3 lots	0/30

Wire Pull	Per Assembly Spec	10x3 lots	0/30
Wedge Shear	Per Assembly Spec	10x3 lots	0/30
CSAM	Per Assembly Spec	60x3lots	0/180
Lead Integrity Test	Tested in the Cascode Qual	--	--
Solderability Test	Tested in the Cascode Qual	--	--

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB and HTGB Burn-In sample size.

FIT = 5.216 failures per billion device hours

MTTF = 21885.5 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha,\nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = {}^{1}/_{\lambda_{hours}}$$

And

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)}$$

Where:

X^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test,

and

k = Boltzmann's Constant.

In our calculations, we used our HTGRB Burn-In data:

D = 231 devices for HTRB,

H = 1000 hours for HTRB,

$1 - \alpha$ = 0.6 (60% Confidence Level)

r = 0 Failures

E_a = 0.7 eV

T_{use} = 55 °C or 328 K

T_{test} = 175 °C or 448 K

United Silicon Carbide, Inc.

Assembly Site Transfer/BoM Change Qualification Report

Discrete TO-247 SiC Stacked Cascode Devices

Included Products:

TO-247-4L	**TO-247-3L**
UF3SC065007K4S	UF3SC120016K3S
UF3SC120009K4S	
UF3SC120016K3S	

This report summarizes the AEC-Q101 qualification results for an Assembly Site Transfer, and a Bill of Materials change for United Silicon Carbide, Inc.'s UF3SC Discrete SiC Cascode in TO-247-3L and TO-247-4L plastic package.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift performance satisfies the AEC-Q101 qualification requirements, as well as UnitedSiC's Quality requirements.

Reliability Stress Test Summary

Test Name	MSL 1 PreCon	Test Standard	# Samples x # Lots	Failures
High Temperature Reverse Bias (HTRB)		JESD22 A108 (1000 Hours) T_J=175°C, V_{GD}=960V, Floating Source	77pcs x 3 lots	0/231
High Temperature Gate Bias (HTGB)		JESD22 A108 (1000 Hours) T_J=175°C, V_{GS}= -20V, V_{DS}= 0V	77pcs x 3 lots	0/231
High Humidity High Temperature Reverse Bias (H3TRB)	Y	JESD22 A-101D (500 Hours) T_A=85°C/85%RH, V_{GD}=100V, Floating source	77x3 lots	0/231
Intermittent Operating Life (IOL)	Y	MIL-STD-750 Method 1037 DT_J ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)	77x3 lots	0/231
Temperature Cycle (TC)	Y	JESD22 A-104 (1000 Cycles) -55°C to +150°C	77x3 lots	0/231
Autoclave (PCT)	Y	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	77x3 lots	0/231
Parametric Verification		Per Datasheet	100% FT x 3 lots	

Physical Dimensions		Per AEC-Q101 Rev D	30x1 packages	0/30
Bondline Thickness		Per Assembly Spec	10x3 lots	0/30
Die Shear		Per Assembly Spec	10x3 lots	0/30
Die Attach Voids		Per Assembly Spec	10x3 lots	0/30
Wire Pull		Per Assembly Spec	10x3 lots	0/30
Wedge Shear		Per Assembly Spec	10x3 lots	0/30
CSAM		Per Assembly Spec	60x3lots	0/180
Lead Integrity Test		Tested in the Cascode Qual	--	--
Solderability Test		Tested in the Cascode Qual	--	--

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB and HTGB Burn-In sample size.

FIT = 2.608 failures per billion device hours

MTTF = 43771 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha, \nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = {}^{1}/_{\lambda_{hours}}$$

And

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)}$$

Where:

X^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test,

and

k = Boltzmann's Constant.

In our calculations, we used our HTGRB Burn-In data:

D = 231 devices for HTRB, and 231 devices for HTGB

H = 1000 hours for HTRB, and HTGB

$1 - \alpha$ = 0.6 (60% Confidence Level)

r = 0 Failures

E_a = 0.7 eV

T_{use} = 55 °C or 328 K

T_{test} = 175 °C or 448 K

United Silicon Carbide, Inc.

Site Transfer Qualification Report

Discrete TO-220-3L 650V Generation 3 Devices

Included Products:

Cascodes:

TO-220-3L

UJ3C065030T3S

UF3C065030T3S

UF3C065040T3S

UJ3C065080T3S

UF3C065080T3S

This report summarizes the Assembly site transfer qualification according to AEC-Q101 guidelines for our Generation 3 Discrete SiC Devices in TO-220-3L plastic packages.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift in performance satisfies the qualification requirements.

Reliability Stress Test Summary

Test Name	Test Standard	# Samples x # Lots	Test Result
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (1000 Hours) T_J=175°C, V=80% V_{max}	77x3 lots	Pass
High Temperature Gate Bias (HTGB)	JESD22 A-108 (1000 Hours) T_J=175°C, V=100% V_{max} (+20V), bias in one direction	77x3 lots	Pass
High Humidity, High Temperature Reverse Bias (H3TRB)	JESD22-A101C (1000 Hours) T_A=85°C, 85% RH, V_{GS}=0V, V_{DS}=100V	77x3 lots	Pass
Temperature Cycle (TC)	JESD22 A-104 -55°C to +150°C 2cycles/Hr (1000 Cycles)	77x3 lots	Pass
Autoclave (PCT)	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	77x3 lots	Pass
Intermittent Operating Life (IOL)	MIL-STD-750 Method 1037 DTJ ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)	77x3 lots	Pass
Parametric Verification	Per Datasheet	100% FT x 3 lots	Pass

United Silicon Carbide, Inc.

Site Transfer Qualification Report

Discrete TO-247-3L/4L 650/1200V Generation 3 Devices

Included Products:

Cascodes & JFETs:

TO-247-3L	TO-247-4L
UF3C170400K3S	UF3C120040K4S
UJ3C120040K3S	UF3C120080K4S
UF3C120040K3S	UF3C120150K4S
UJ3C120070K3S	UF3C065030K4S
UJ3C120080K3S	UF3C065040K4S
UF3C120080K3S	UF3C065080K4S
UJ3C120150K3S	
UF3C120400K3S	
UJ3C065030K3S	
UF3C065030K3S	
UF3C065040K3S	
UJ3C065080K3S	
UF3C065080K3S	
UJ3N120035K3S	
UJ3N120065K3S	
UJ3N120070K3S	
UJ3N065025K3S	
UJ3N065080K3S	
UF3N120008K3S	

Diodes:

TO-247-3L
UJ3D1210KS
UJ3D1210KSD
UJ3D1220KSD
UJ3D06520KSD
UJ3D06560KSD

This report summarizes the Assembly site transfer qualification according to AEC-Q101 guidelines for our Generation 3 Discrete SiC Devices in TO-247-3L and TO-247-4L plastic packages.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift in performance satisfies the qualification requirements.

Reliability Stress Test Summary

Test Name	Test Standard	# Samples x # Lots	Failures
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (1000 Hours) T_J=175°C, V=80% V_{max}	77x3 lots	0/231
High Temperature Gate Bias (HTGB)	JESD22 A-108 (1000 Hours) T_J=175°C, V=100% V_{max} (+20V), bias in one direction	77x3 lots	0/231
High Humidity, High Temperature Reverse Bias (H3TRB)	JESD22-A101C (1000 Hours) T_A=85°C, 85% RH, V_{GS}=0V, V_{DS}=100V	77x3 lots	0/231
Temperature Cycle (TC)	JESD22 A-104 -55°C to +150°C 2cycles/Hr (1000 Cycles)	77x3 lots	0/231
Autoclave (PCT)	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	77x3 lots	0/231
Intermittent Operating Life (IOL)	MIL-STD-750 Method 1037 DTJ ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)	77x3 lots	0/231
Parametric Verification	Per Datasheet	100% FT x 3 lots	
Physical Dimensions	Per AEC-Q101 Rev D	30x1 packages	0/30
Bondline Thickness	Per Assembly Spec	10x3 lots	0/30

Die Shear	Per Assembly Spec	10x3 lots	0/30
Die Attach Voids	Per Assembly Spec	10x3 lots	0/30
Wire Pull	Per Assembly Spec	10x3 lots	0/30
Wedge Shear	Per Assembly Spec	10x3 lots	0/30
CSAM	Per Assembly Spec	60x3 lots	0/180
Lead Integrity Test	Per AEC-Q101 Rev D	30x1 lots	0/30
Solderability Test	Per AEC-Q101 Rev D	10x1 lots	0/10

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB and HTGB Burn-In sample size.

FIT = 2.608 failures per billion device hours

MTTF = 43771.03 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha, \nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = {}^{1}/_{\lambda_{hours}}$$

And

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)}$$

Where:

X^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test,

and

k = Boltzmann's Constant.

In our calculations, we used our HTGB and HTRB Burn-In data:

D = 231 for HTRB, and 231 for HTGB

H = 1000 hours of HTRB, and 1000 hours of HTGB

$1 - \alpha$ = 0.6 (60% Confidence Level)

r = 0 Failures

E_a = 0.7 eV

T_{use} = 55 °C or 328 K

T_{test} = 175 °C or 448 K