



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-PWR/10/5337
Notification Date 02/01/2010

SILICON LINE CHANGE FOR BIPOLAR DEVICES - BB04 PRODUCT LINE

Table 1. Change Implementation Schedule

Forecasted implementation date for change	26-Apr-2010
Forecasted availability date of samples for customer	25-Jan-2010
Forecasted date for STMicroelectronics change Qualification Plan results availability	25-Jan-2010
Estimated date of changed product first shipment	03-May-2010

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Waferfab process change
Reason for change	Production Optimization
Description of the change	Planar Base Island technology is ready to replace the mature Epibase technology in order to align our products to the actual Market. The line BB04 will replace the old ones B513. Feature: Improved hFE linearity and Higher fT frequency. Benefit: Better performances in switching and linear application.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	See "N" in additional info
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
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Reliability evaluation on BB04 for silicon line change

General Information	
Product Line	BB04
Product Description	NPN POWER DARLINGTON TRANSISTOR
P/N	TIP142
Product Group	01 - APM
Product division	12 - PWR BIP/ IGBT/ RF
Package	TO-247
Silicon Process technology	PLANAR NPN

Locations	
Wafer fab	AMK - SINGAPORE
Assembly plant	LONGGANG
Reliability Lab	IMS – CATANIA

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Jan-2010	6	G.Montalto	G.Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To evaluate a new LV NPN Planar transistor in monolithic Darlington configuration.

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



4 DEVICE CHARACTERISTICS

4.1 Device description

The TIP142 is a silicon Planar NPN transistor in monolithic Darlington configuration intended for use in power linear and switching application.

4.2 Construction note

D.U.T.: TIP142 LINE: BB04

Wafer/Die fab. information	
Wafer fab manufacturing location	<i>Ang Mo Kio (SINGAPORE)</i>
Technology	PLANAR NPN
Die finishing back side	AuAs-Cr-Ni-Au
Die size	3560 um x 3290 um
Metal 1	Al/Si
Passivation type	PSG

Wafer Testing (EWS) information	
Electrical testing manufacturing location	<i>Ang Mo Kio (SINGAPORE)</i>
Test program	WPIS

Assembly information	
Assembly site	LONGGANG
Package description	TO-247
Molding compound	Epoxy resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	95.5%(Pb) / 2%(Sn) / 2.5%(Ag)
Wire bonding process	Ultrasonic
Wires bonding materials/diameters	Al/Mg Base / 5 mils Al Emitter / 10 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	LONGGANG
Tester	IP test



5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Process/ Package	Product Line	Comments
1	W904J23	TO-247	BB04	Power BIPOLAR
2				
3				

5.2 Test plan and results summary

D.U.T.: TIP142 LINE: BB04

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
HTSL	N	JESD22 A-103	Ta = 150°C	77	1000H	0/77
HTRB	N	JESD22 A-108	T.A.=150°C Vdd=80V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdd=100V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-65°C TO 150°C	77	500 cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77
TF	N	JESD22 A-105-B	ΔTC=70°C - Pd=24W	77	10Kcy.	0/77



6 ANNEXES

ANNEXES 6.0

6.1 Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: <ul style="list-style-type: none">• low power dissipation;• max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF Thermal Fatigue	This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress).	The purpose of this test is to detect assembly defects: improper die-attach, bonding weakness and thermal mismatch among various components of the package.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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