



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MIC/08/3483
Notification Date 02/25/2008

CMOSM6XT/DT PROCESS TECHNOLOGY TRANSFER TO CATANE M5 (ITALY)

MIC - MICROCONTROLLERS

Table 1. Change Implementation Schedule

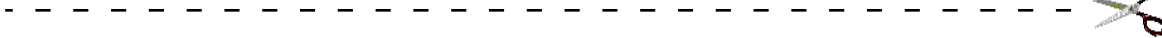
Forecasted implementation date for change	18-May-2008
Forecasted availability date of samples for customer	18-May-2008
Forecasted date for STMicroelectronics change Qualification Plan results availability	18-May-2008
Estimated date of changed product first shipment	19-May-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See page 5
Type of change	Waferfab location change
Reason for change	Phoenix fab closure
Description of the change	Add Catane M5 fab (Italy) as a qualified wafer fab. All datasheet parameters are identical to Phoenix silicon.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Package marking from "VP" to "V5"
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN MMS-MIC/08/3483
Please sign and return to STMicroelectronics Sales Office		Notification Date 02/25/2008
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name: _____	
	Title: _____	
	Company: _____	
	Date: _____	
	Signature: _____	
Remark		

DOCUMENT APPROVAL

Name	Function
Colonna, Daniel	Division Marketing Manager
Nicholas, Jimmy Edward	Division Product Manager
Narche, Pascal	Division Q.A. Manager

Impacted Part Number			
ST72F321AR6T3	ST72F324J2T6	ST72F32AJ2T6	ST72F621L4M1
ST72F321AR6T6	ST72F324J2T6TR	ST72F32AK1B6	ST72F622L2M1
ST72F321AR7T6	ST72F324J4B5	ST72F32AK1T6	ST72F622L2M1TR
ST72F321AR7T6TR	ST72F324J4B6	ST72F32AK1T6TR	ST72F623F2B1
ST72F321AR9T3	ST72F324J4T6	ST72F32AK2B6	ST72F623F2M1
ST72F321AR9T6	ST72F324J4T6/TR	ST72F32AK2T6	ST72F623F2M1TR
ST72F321AR9T6TR	ST72F324J6B5	ST72F32HPJ2T1	ST72F63BD6U1
ST72F321BAR6T6	ST72F324J6B6	ST72F361AR6T3	ST72F63BD6U1TR
ST72F321BAR7T6	ST72F324J6T3	ST72F361AR6T6	ST72F63BE1M1
ST72F321BAR9T3	ST72F324J6T3TR	ST72F361AR7T3	ST72F63BE2M1
ST72F321BAR9T6	ST72F324J6T5	ST72F361AR7T6	ST72F63BE4M1
ST72F321B/DIE6	ST72F324J6T6	ST72F361AR9T3	ST72F63BE6M1
ST72F321BJ6T3	ST72F324J6T6E	ST72F361AR9T6	ST72F63BH2T1
ST72F321BJ6T6	ST72F324J6T6/TR	ST72F361J6T3	ST72F63BH4T1
ST72F321BJ6T6TR	ST72F324K2B6	ST72F361J6T6	ST72F63BH6T1
ST72F321BJ7T6	ST72F324K2T3	ST72F361J7T3	ST72F63BK1B1
ST72F321BJ7T6TR	ST72F324K2T3TR	ST72F361J7T6	ST72F63BK1M1
ST72F321BJ9T3	ST72F324K2T6	ST72F361J9T3	ST72F63BK2B1
ST72F321BJ9T6	ST72F324K4B6	ST72F361J9T6	ST72F63BK2M1
ST72F321BK6T6	ST72F324K4T6	ST72F361K6T3	ST72F63BK2U1
ST72F321BK6T6TR	ST72F324K4T6TR	ST72F361K6T6	ST72F63BK2U1TR
ST72F321BR6T6	ST72F324K6B5	ST72F361K7T3	ST72F63BK4M1
ST72F321BR7T6	ST72F324K6B6	ST72F361K7T6	ST72F63BK6B1
ST72F321BR7T6TR	ST72F324K6T3	ST72F361K9T3	ST72F63BK6M1
ST72F321BR9T3	ST72F324K6T6	ST72F361K9T6	ST72F651AR6T1
ST72F321BR9T6	ST72F324K6T6/TR	ST72F521AR6T6	ST72F651AR6T1E
ST72F321J7T6	ST72F324LJ2T5	ST72F521AR9T6	ST72P321AR9/NOL
ST72F321J7T6TR	ST72F324LJ2T5TR	ST72F521M9T3	ST72P324BT/NXCTR
ST72F321J9T3	ST72F324LJ2T6	ST72F521M9T6	ST72P324BT/ONUTR
ST72F321J9T3TR	ST72F324LJ4T6	ST72F521M9T6TR	ST72P325T5/OARTR
ST72F321J9T6	ST72F324LJ4T6TR	ST72F521R6T6	ST7FMC1K2T3
ST72F321M6T6	ST72F324LJ6B6	ST72F521R9T3	ST7FMC1K2T6
ST72F321M9T6	ST72F324LJ6T6	ST72F521R9T6	ST7FMC1K2T6/TR
ST72F321R6T6	ST72F324LK2T6	ST72F561AR4T6	ST7FMC1K4T3
ST72F321R6T6TR	ST72F324LK4T6	ST72F561AR6T3	ST7FMC1K4T6
ST72F321R9T6	ST72F324LK6B5	ST72F561AR7T6	ST7FMC2M6T6
ST72F324BJ2B6	ST72F324LK6B6	ST72F561AR9T3	ST7FMC2M9T6
ST72F324BJ2T6	ST72F324LK6T6	ST72F561AR9T6	ST7FMC2N6B6
ST72F324BJ4B5	ST72F324LS2T6	ST72F561J4T6	ST7FMC2R6T6
ST72F324BJ4B6	ST72F324LS4T6	ST72F561J6T6	ST7FMC2R7T6
ST72F324BJ4T3	ST72F325AR6T6	ST72F561J7T6	ST7FMC2R7T6TR
ST72F324BJ4T6	ST72F325AR9T6	ST72F561J9T3	ST7FMC2S4T3
ST72F324BJ4T6TR	ST72F325J4T6	ST72F561J9T6	ST7FMC2S4T6
ST72F324BJ6B5	ST72F325J4T6TR	ST72F561K4T6	ST7FMC2S6T3
ST72F324BJ6B6	ST72F325J6B6	ST72F561K6T6	ST7FMC2S6T6
ST72F324BJ6T3	ST72F325J6T3	ST72F561K7T6	ST7FMC2S7T6
ST72F324BJ6T6	ST72F325J6T6	ST72F561K9T3	ST7FSCR1E4M1
ST72F324BJ6T6TR	ST72F325J7T3TR	ST72F561K9T6	ST7FSCR1E4M1TR
ST72F324BK2B6	ST72F325J7T6	ST72F561R6T3	ST7FSCR1R4T1
ST72F324BK2T3	ST72F325J7T6TR	ST72F561R9T3	ST7MDT20-CHIP
ST72F324BK2T3TR	ST72F325J9T6	ST72F561R9T6	ST7MDTU3B-CHIP
ST72F324BK2T6	ST72F325K4T3TR	ST72F60E1M1	ST7PMC1K2/OCJTR
ST72F324BK2T6TR	ST72F325K4T6	ST72F60E2M1	ST7PMC2R7/OIFTR
ST72F324BK4B6	ST72F325K4T6TR	ST72F60K1U1TR	ST7PMC2R7/OPFTR
ST72F324BK4T3	ST72F325K6B6	ST72F60K2B1	ST7PSCR1M1/NXH
ST72F324BK4T3TR	ST72F325K6T3	ST72F60K2DIE1	ST7PSCR1M1OOSTR
ST72F324BK4T6	ST72F325K6T6	ST72F60K2DIE6	ST7PSCR1M1/OPX
ST72F324BK4T6TR	ST72F325K6T6TR	ST72F60K2U1	ST7PSCR1M1ORHTR
ST72F324BK6B6	ST72F325R9T6	ST72F60K2U1TR	ST7PSCR1T1/OCU
ST72F324BK6T3	ST72F32AJ1B6	ST72F621J4B1	ST7PSCR1T1OHCTR
ST72F324BK6T6	ST72F32AJ1T6	ST72F621J4T1	
ST72F324J2B6	ST72F32AJ2B6	ST72F621K4B1	

CMOSM6X-T & CMOSM6D-T PRODUCT VEHICLES

**2 TEST VEHICLES WILL ALLOW TO QUALIFY
CMOSM6X-T & CMOSM6D-T PROCESS IN CATANIA M5**

	CMOSM6X-T	CMOSM6D-T
TEST VEHICLE	ST72F521	ST72F561
DIE NAME	813	832
PACKAGE ASSEMBLY SITE	TQFP64 14*14 MUAR	TQFP64 14*14 MUAR
QUALIFICATION LOTS	1 LOT	2 LOTS
RELIABILITY DURATION	14 weeks (1)	15 weeks (1)

(1) + 4 weeks for EWS, Assy and FT after qual lot Fab out date



CMOSM6X/D-T – RELIABILITY PLAN (1/3)

DIE ORIENTED RELIABILITY TRIALS

TEST	SPECIFICATIONS	NUMBER OF PARTS	ACCEPTANCE CRITERIA
ESD (Human Body Model)	AEC Q100 Method 002	6 PARTS / product	1500 Ω , 100 pF 2000 V / All leakage < 1 μ A
ESD (Charge Device Model)	AEC Q100 Method 003	6 PARTS / product	0 Ω , 200 pF 500 V / All leakage < 1 μ A
LATCH UP	AEC Q100 Method 004	6 PARTS / product	Overstress limits at 1.5 x VDDmax or 100 mA @ 125°C



CMOSM6X/D-T – RELIABILITY PLAN (2/3)

DIE ORIENTED RELIABILITY TRIALS

TEST	SPECIFICATIONS	NUMBER OF PARTS			ACCEPTANCE CRITERIA
		LOT 1	LOT 2	LOT 3	
EARLY FAILURE RATE (1)	AEC Q100 Method 008	500	500	500	24 HRS / 140°C / 6V No reject with std Final Test
HIGH TEMPERATURE OPERATING LIFE TEST (1)	MIL Std 883E Method 1005	77	77	77	500 HRS / 140°C / 6V No reject with std Final Test
HIGH TEMPERATURE RETENTION BAKE (1)	MIL Std 883E Method 1008	77	77	77	1000 HRS / 175°C / No Bias No reject with std Final Test
EEPROM ENDURANCE CYCLING + POST RETENTION BAKE	ADCS 0061692	77	77	77	300 CYCLES @ 25°C + BAKE 72 HRS @ 175°C No reject with std Final Test
FLASH ENDURANCE CYCLING (at Hot /Cold temp) + POST RETENTION BAKE	ADCS 0061692	77	77	77	100 CYCLES @ 85° / -40°C + BAKE 72 HRS @ 175°C No reject with std Final Test

(1) PRECONDITIONING IS PERFORMED PRIOR TO THIS TRIAL



CMOSM6X/D-T – RELIABILITY PLAN (3/3)

PACKAGE ORIENTED RELIABILITY TRIALS

TEST	SPECIFICATIONS	NUMBER OF PARTS	ACCEPTANCE CRITERIA
		1 LOT	
EXTERNAL VISUAL	JB 101	ALL	DATASHEET PACKAGE SPECIFICATIONS
PRECONDITIONING	JEDEC J-STD-20	300	JEDEC LEVEL 3
TEMPERATURE AND HUMIDITY BIAS (1)	CECC 90000	77	1000 HRS / 85°C / 85% R.H. / 5.5V
THERMAL CYCLING (1)	Mil Std 883E Method 1010	77	1000 CYCLES / -40°C TO 150°C
PRESSURE POT (1)	JA 102	77	240 HRS / 121°C / 2 ATM / 100% R.H.

(1) PRECONDITIONING WILL BE DONE ON THB, TMCL AND PPOT PARTS



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