



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/07/2861
Notification Date 08/31/2007

**M24C04-W (2.5V to 5.5V Vcc range), 4Kbit Serial I2C Bus
EEPROM Redesign and Die Optimization**

MMY - MEMORY

Table 1. Change Identification

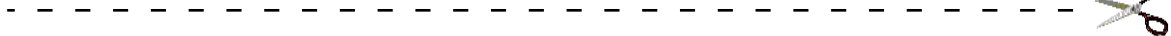
Product Identification (Product Family/Commercial Product)	M24C04-W (2.5V to 5.5V Vcc range)
Type of change	Product design change
Reason for change	Production capacity increase and line up to state of the art of low voltage
Description of the change	New design
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process Technology/Wafer fab identifier is "Q" for the redesigned version
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

Forecasted implementation date for change	03-Sep-2007
Forecasted availability date of samples for customer	24-Aug-2007
Forecasted date for STMicroelectronics change Qualification Plan results availability	24-Aug-2007
Estimated date of changed product first shipment	05-Nov-2007

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN MMS-MMY/07/2861					
Please sign and return to STMicroelectronics Sales Office		Notification Date 08/31/2007					
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="padding: 2px;">Name:</td></tr> <tr><td style="padding: 2px;">Title:</td></tr> <tr><td style="padding: 2px;">Company:</td></tr> <tr><td style="padding: 2px;">Date:</td></tr> <tr><td style="padding: 2px;">Signature:</td></tr> </table>		Name:	Title:	Company:	Date:	Signature:
Name:							
Title:							
Company:							
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DOCUMENT APPROVAL

Name	Function
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Yackowlew, Nicolas	Division Q.A. Manager



PRODUCT / PROCESS CHANGE NOTIFICATION

M24C04-W (2.5V to 5.5V Vcc range), 4Kbit Serial I²C Bus EEPROM Redesign and Die Optimization

What is the change?

The M24C04-W (Vcc 2.5V to 5.5V) 4 Kbit I²C bus Serial EEPROM device, processed in the CMOSF6SP/DM (Single Poly/Double Metal) 36% shrink Process Technology and currently produced in the ST AMK (Singapore) 6 inch wafer diffusion plant, has been redesigned for improved performances using the same Process Technology in the same wafer diffusion plant.

Why?

The strategy of STMicroelectronics Memory division is to support the growth of our customers on a long-term basis. In line with this commitment, the qualification of the redesigned M24C04 die in the same CMOSF6SP/DM Process Technology will increase the production capacity throughput, reduce the lead-time and consequently improve the service to our customers.

When?

Production will ramp up from September 2007 and shipments will start from November 2007 onward. The phase out of the current version will start from November 2007 with a completion planned for Q1 2008.

How will the change be qualified?

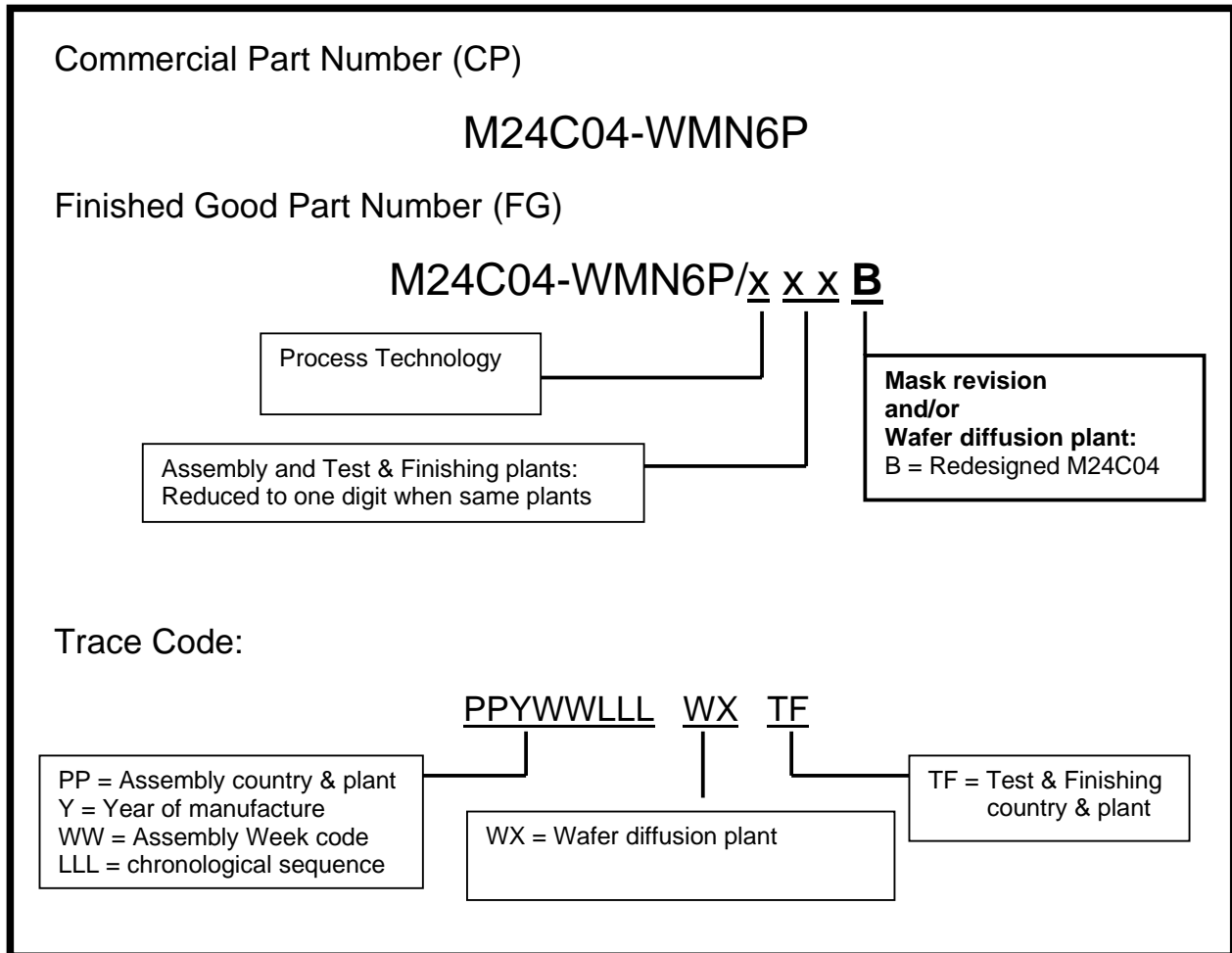
The new version of the M24C04 has been qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability. The qualification report QREE0524 is available.

How can the change be seen?

- BOX LABEL MARKING

On the BOX LABEL MARKING, the change is visible inside the Finished Good Part Number: the **Mask revision and/or Wafer diffusion plant** identifier is “**B**” for the **redesigned version**, the identifier being “**A**” for the current version.

→ Example for M24C04-WMN6P (2.5V to 5.5V Vcc range, SO8N RoHS* compliant package)



*RoHS: Restriction of the use of certain Hazardous Substances in electrical and electronic equipments

How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the SO8N package, the change is visible on the top side marking, inside the second line of the trace code (PYWWT): the last digit "T" for the **Process Technology/wafer fab** identifier is "**Q**" for the **redesigned version**, the identifier being "**G**" for the current version.



The traceability for each device is as follows:

PYWWT

P = Assembly country & plant
Y = Last digit of the Year of Assembly
WW = Assembly Week code
T = Process Technology / Wafer Fab

For the TSSOP8 package, for package size reason, the change is only visible inside the Finished Good Part Number appearing on the BOX LABEL MARKING (See "Mask Revision and/or Wafer diffusion plant" identifier on previous page).

Appendix A- Product Change Information

Product family / Commercial products:	M24C04-W (2.5V to 5.5V Vcc range)
Customer(s):	All
Type of change:	Redesign and die optimization
Reason for the change:	Production capacity increase and line up to state of the art of low voltage design
Description of the change:	New design
Forecast date of the change:	September 2007
Forecast availability date of qualification sample for the customer(s):	Available
Forecast date for the internal STMicroelectronics change, Qualification report availability:	Available
Marking to identify the changed product:	Process Technology/Wafer fab identifier is "Q" for the redesigned version
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	M24C04-WMN6P - M24C04-WMN6TP M24C04-WDW6TP M24C04-WBN6P
Manufacturing location:	ST AMK (Singapore) 6 inch wafer fab
Estimated date of first shipment:	November 2007
Division Product Manager: B. RODRIGUES	Date:
Group QA Manager: N. YACKOWLEW	Date:

APPENDIX B: Qualification Plan:

PRODUCT DESCRIPTION

	Device to qualify	Qualified similar device
Product name	M24C04GB / M24C08GB	M24C16GA
	(same mask set)	
Memory size	4Kb/8Kb	16Kb

SIMILARITY

The CMOSF6SPDM 36% Process Technology is already qualified in ST Ang Mo Kio 6 inch wafer fab with the M24C16G (QREE0320) which has a larger or equivalent memory array.

CHARACTERIZATION

Table 1. Characterization requirements.

Number of lots	Parameters	Vcc range	Temperature range
3	All	1.8V/5.5V	-40°C/85°C

RELIABILITY

Table 2. Product qualification. Die-related reliability tests

EEPROM

Sub-group	Test Procedure	Method	Test Conditions	Num of Lots	Criteria ⁽¹⁾
1	Erase/Write Cycles and HTOL	AEC-Q100-005	100,000 E/W cycles at 125°C, 1000 hrs HTOL 150°C	1	0/77
2	Erase/Write Cycles and Bake	AEC-Q100-005	100,000 E/W cycles at 125°C, 1000 hrs Bake 150°C	1	0/77
3	High Temperature Bake	AEC - Q100 - JA 103	200°C, 1000 hrs	1	0/77
4	Erase/Write Cycles and Bake	Internal	1,000,000 E/W cycles Bake: 200°C, 48 hrs	1	0/77
5	Electrostatic Discharge	AEC - Q100 - 002 & 003	Human body model: 1.5kΩ 100pF Machine Model: 200pF	1 by product ⁽²⁾	0/9
6	Latch-Up	AEC - Q100 - 004	At 150°C (Class II - Level A)	1 by product ⁽²⁾	0/6

(1) The notation 0/77 means: accepted with 0 reject out of 77 units (rejected with 1 reject)

(2) The M24C04GB is derived from the M24C08GB by a metal option. Therefore, only ESD and Latch-Up tests will be performed on the M24C04GB since the qualification is mainly based on M24C08GB results.

Document Revision History		
Date	Rev.	Description of the Revision
May 03, 2007	1.00	First draft creation (Christian POLI)

Source Documents & Reference Documents		
Source document Title	Rev.:	Date:

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