



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/07/2730
Notification Date 07/16/2007

**M93C46, 1Kbit Serial Microwire Bus EEPROM Redesign and
Die Optimization - Updates & replaces PCN MMS-SNV/07/2580**

MMY - MEMORY

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	M93C46 products family
Type of change	Product design change
Reason for change	Die optimization
Description of the change	New design
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Wafer fab identifier is "Q" for the new version
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

Forecasted implementation date for change	15-Aug-2007
Forecasted availability date of samples for customer	09-Jul-2007
Forecasted date for STMicroelectronics change Qualification Plan results availability	15-Aug-2007
Estimated date of changed product first shipment	15-Oct-2007

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN MMS-MMY/07/2730
Please sign and return to STMicroelectronics Sales Office		Notification Date 07/16/2007
<input type="checkbox"/> Qualification Plan Denied	Name:	
<input type="checkbox"/> Qualification Plan Approved	Title:	
<input type="checkbox"/> Change Denied	Company:	
<input type="checkbox"/> Change Approved	Date:	
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DOCUMENT APPROVAL

Name	Function
Poli, Christian	Division Marketing Manager
Rodrigues, Benoit	Division Product Manager
Yackowlew, Nicolas	Division Q.A. Manager



PRODUCT / PROCESS CHANGE NOTIFICATION

M93C46, 1Kbit Serial Microwire Bus EEPROM Redesign and Die Optimization

Updates & replaces PCN MMS-SNV/07/2580

What is the change?

The M93C46, 1Kbit Serial Microwire Bus EEPROM product family, produced in the CMOSF6SP36% DM Process Technology, will be redesigned and optimized using the same Process Technology in the ST AMK 6 (Singapore) wafer diffusion plant.

Only M93C46-Wxxx (2.5V-5.5V Vcc range) sales codes are concerned. The current 1.8V-5.5V Vcc range version is not concerned by this change.

Why?

The strategy of STMicroelectronics Memory Division is to support the growth of our customers on a long-term basis. In line with this commitment, the qualification of the redesigned M93C46 die will increase the production capacity throughput, reduce the lead-time and consequently improve the service to our customers.

When?

The production of the new M93C46 will ramp up from August 2007 and shipments will start from September 2007 onward.

The phase out of the current version of the M93C46 Serial EEPROM will start from August 2007 with a phase out completion planned for October 2007.

How will the change be qualified?

The new version of the M93C46 will be qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

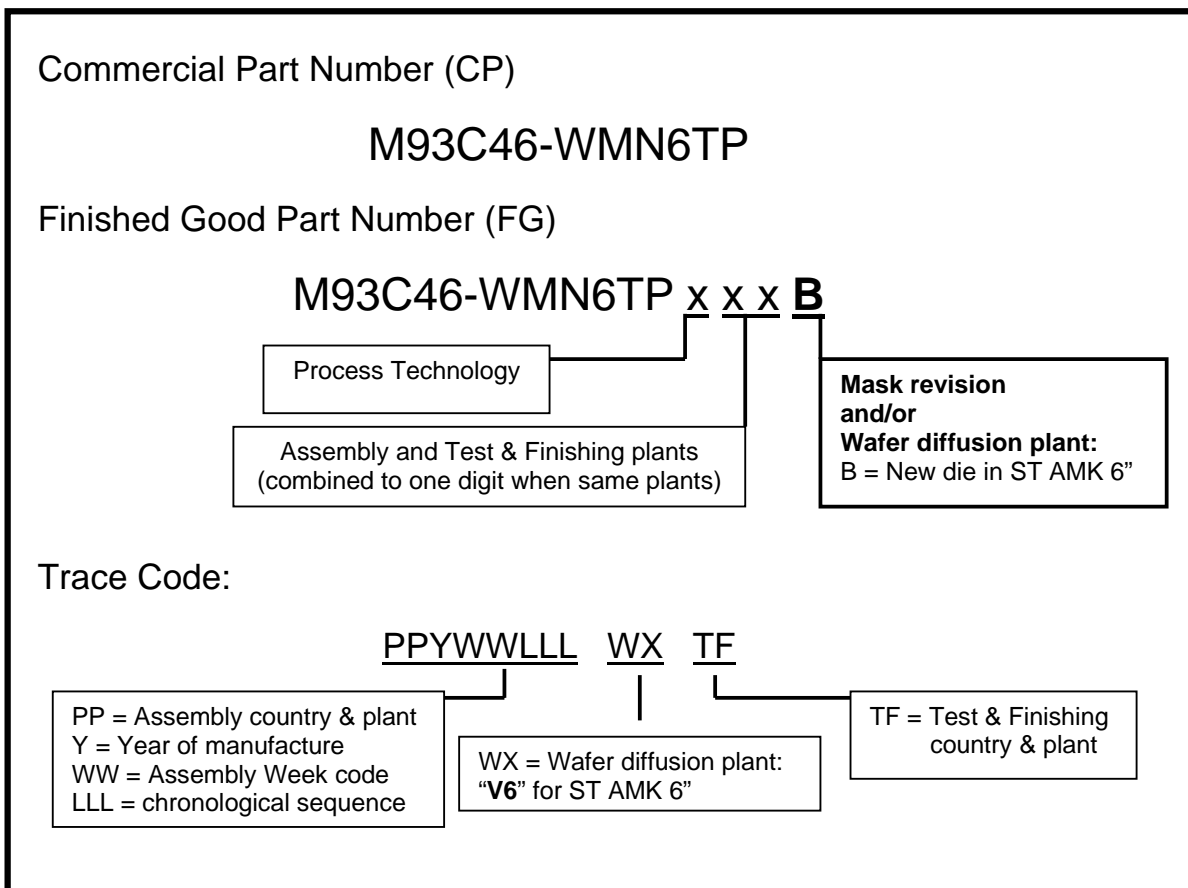
The qualification report QREE0701 will be available in August 2007.

How can the change be seen?

- BOX LABEL MARKING

The change is only visible on the BOX LABEL MARKING, inside the Finished Good Part Number: the **Mask revision and /or Wafer diffusion plant** identifier is “**B**” for the **redesigned version**, the identifier being “**A**” for the previous version.

➔ Example for M93C46-WMN6TP (2.5V to 5.5V Vcc range, SO8N RoHS* compliant package)



*RoHS: Restriction of the use of certain Hazardous Substances in electrical and electronic equipments

Appendix A- Product Change Information

Product family / Commercial products:	M93C46 products family
Customer(s):	All
Type of change:	Redesign and die optimization
Reason for the change:	Die optimization
Description of the change:	New design
Forecast date of the change:	August 2007
Forecast availability date of qualification sample for the customer(s):	Available
Forecast date for the internal STMicroelectronics change, Qualification report availability:	August 2007
Marking to identify the changed product:	Wafer fab identifier is "Q" for the new version
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See list of concerned products in appendix B
Manufacturing location:	ST AMK (Singapore) 6 inch wafer fab
Estimated date of first shipment:	September 2007
Division Product Manager: B. RODRIGUES	Date: Jul. 09, 2007
Group QA Manager: N. YACKOWLEW	Date: Jul. 06, 2007

Appendix B: concerned products:

M93C46-WMN6P
M93C46-WMN6TP
M93C46-WBN6P
M93C46-WDW6TP

Appendix C: Qualification Plan:

PRODUCT DESCRIPTION

	Device to qualify	Qualified similar device
Product name	M93C46GB	M93C46GA / M24C02W & M24C01W for qual packages
Memory size	1K	1K / 2K

SIMILARITY

The CMOSF6SP36%DM Process Technology is already qualified in ST AMK6" wafer diffusion plant. The M24C01W & M24C02W are already qualified using scribe line 80um & BPO 80x80um.

CHARACTERIZATION

Table 1. Characterization requirements.

Number of lots	Parameters	Vcc range	Temperature range
3	All	2.5V/5.5V	-40°C/85°C

RELIABILITY

Table 2. Product qualification. Die-related reliability tests

EEPROM

Abrv.	Test Procedure	Method	Test Conditions	Num of lots	Criteria
EDR	NVM Endurance	AEC-Q100-005	1Myc @25C or 100Kcyc @125C cycles, then: - HTSL 150°C, 1000 hrs - HTOL 150°C, 1000 hrs	1 1	0/80 0/80
HTB	High Temperature Bake	Internal	200°C, 1000 hrs	1	0/80
LTOL	Low Temperature Operating Life	Mil Std 883 Method 1005	-40°C, VCC+20%, 1000 hrs	1	0/80
W/E	Erase/Write cycles and Bake	Internal.	Up to 10M E/W cycles Bake: 200°C, 48hr	1	0/80
ESD HBM	Electrostatic Discharge	AEC-Q100-002	Human Body Model: 1.5k , 100pF : Up to 4500V (step 500V)	1	0/81
ESD MM	Electrostatic Discharge	AEC-Q100-003	Machine Model: 0k , 200pF, 250V & 400V	1	0/18
LU	Latch-up	AEC-Q100-004	Class II Level A (Max operating temperature)	1	0/6

Table 3. Product qualification. Package-related reliability tests (SO8N/ TSSOP8/ PDIP8 package)

Test Procedure	Method	Test Conditions	Num of lots	Criteria
Preconditioning	AEC - Q100 - J-STD-020C	Level 1 for EEPROM	1 *	0 fail
Pressure Pot	AEC - Q100 - JA 102 JESD22-A102	121°C, 2atm, 100% RH, 168 hrs	1 *	0/80
Temperature and Humidity Bias	AEC - Q100 - JA 101 JESD22-A101	85°C, 85% RH, 5.5V, 1000 hrs	1 *	0/80
High Temperature Bake	AEC - Q100 JA 103 JESD22-A103B	150°C, 1000hrs	1 *	0/80
Temperature Cycling	AEC - Q100 - JA 104 JESD22-A104B	-65°C / 150°C, 1000 cycles	1 *	0/80
Thermal Shock	Mil Std 883 Method 1011B JESD22-A106B	-55°C / 125°C, 200 shocks	1 *	0/25
Electrostatic Discharge CDM	AEC-Q100-011	Charge Device Model (Field Induced CDM) : Up to 1500V (step 250V)	1 by product	0/18

* No package qualification needed. All reliability trials and package qualification already performed on devices using same technology with higher densities.

Document Revision History		
Date	Rev.	Description of the Revision
Jun. 20, 2007	1.00	First draft creation
		Signed off B. RODRIGUES
		Signed off N. YACKOWLEW

Source Documents & Reference Documents		
Source document Title	Rev.	Date
PCN MMS-SNV/07/2580	1.00	May 2007

Changes from PCN MMS-SNV/07/2580
- Delivery planning update
- Change definition clarification

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