



# PRODUCT/PROCESS CHANGE NOTIFICATION

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PCN APM-PMT/07/2634  
Notification Date 06/27/2007

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**New Additional Assy-Testing to Subcontract PSI (Taguig,  
Philippines) for Package: D2PAK**

**PMT - POWER MOSFET**

**Table 1. Change Identification**

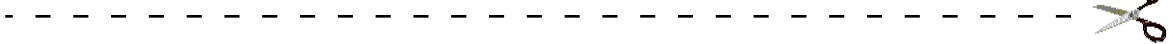
Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly location change
Reason for change	Capacity Extension
Description of the change	Devices in D2PAK will be manufactured also in Subcontractor PSI (Taguig, Philippines)
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	1st two digits of the traceability code are 7P
Manufacturing Location(s)	

**Table 2. Change Implementation Schedule**

Forecasted implementation date for change	04-Sep-2007
Forecasted availability date of samples for customer	20-Jun-2007
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	20-Jun-2007
Estimated date of changed product first shipment	26-Sep-2007

**Table 3. List of Attachments**

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN APM-PMT/07/2634
Please sign and return to STMicroelectronics Sales Office		Notification Date 06/27/2007
<input type="checkbox"/> Qualification Plan Denied	Name:	
<input type="checkbox"/> Qualification Plan Approved	Title:	
<input type="checkbox"/> Change Denied	Company:	
<input type="checkbox"/> Change Approved	Date:	
	Signature:	
Remark	..... ..... ..... ..... ..... ..... ..... ..... ..... ..... .....	

## DOCUMENT APPROVAL

Name	Function
Giudice, Maurizio	Division Marketing Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

# PACKAGE DIMENSIONAL COMPARISON

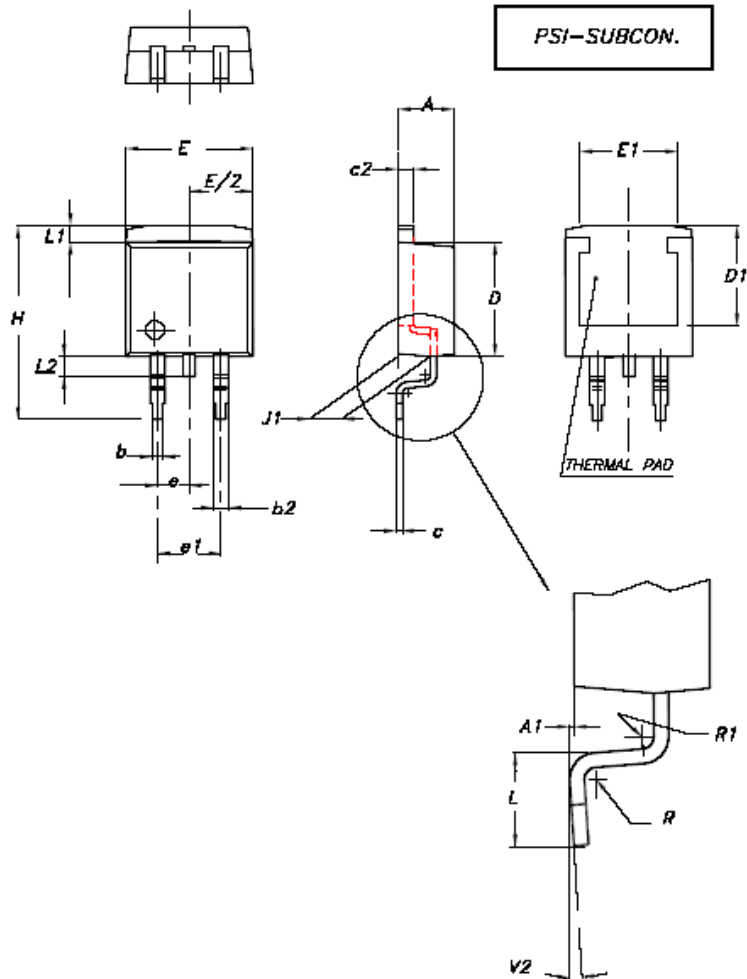
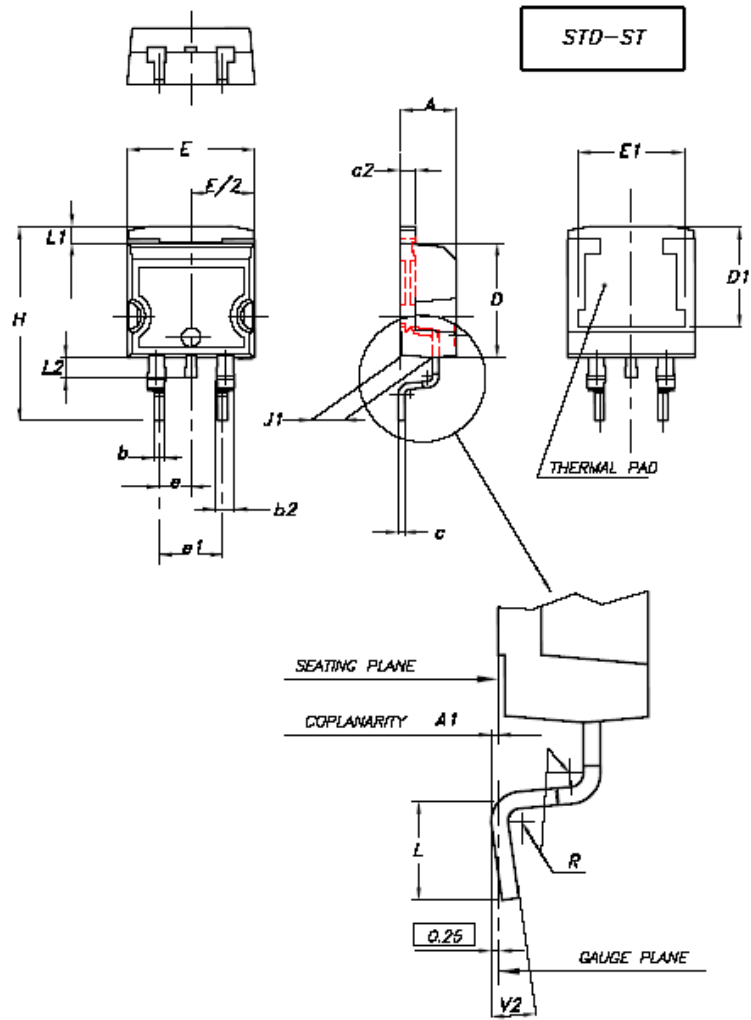
## D2PAK

### ST – PSI SUBCONTRACTOR

STD-ST D2PAK DIMENSIONS				PSI SUBCON. D2PAK DIMENSIONS			
DATA BOOK mm (NOTE)				DATA BOOK mm (NOTE)			
REF	NOM	MIN	MAX	REF	NOM	MIN	MAX
A		4.40	4.60	A		4.32	4.57
A1		0.03	0.23	A1	0.127	0.00	0.254
b		0.70	0.93	b		0.76	0.87
b2		1.14	1.70	b2		1.21	1.58
c		0.45	0.60	c	0.38 (5)	0.33 (5)	0.44 (5)
c2		1.23	1.36	c2	1.27	1.22	1.32
D		8.95	9.35	D	8.64	8.50	8.77
D1		7.50 (1)		D1		7.46 (1)	7.77 (1)
E		10	10.40	E		10	10.32
E1		8.50 (1)		E1		7.54 (1)	7.70 (1)
e	2.54			e	2.54		
e1		4.88	5.28	e1	5.08		
H		15	15.85	H	15.37	15.11	15.62
J1		2.49	2.69	J1		2.61	2.72
L		2.29 (2)	2.79 (2)	L		2.28 (2)	2.79 (2)
L1		1.27	1.40	L1		1.44	1.60
L2		1.30	1.75	L2		1.27 (3)	1.78 (3)
R	0.4			R	0.51		
				R1	0.76		
V2		0°	8°	V2		0°	5°

#### GENERAL PACKAGE PERFORMANCE

- 1 – “D1” and “E1” dimensions establish a minimum mounting surface for thermal pad.
- 2 – “L” is the terminal length for soldering.
- 3 – Solder finish uncontrolled in this area..
- 5 – “c” dimension a jedec is MIN 0.38



	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

**RELIABILITY EVALUATION**

**ON**

**PSI NEW ADDITIONAL ASSEMBLY**

**LOCATION FOR PACKAGE D<sup>2</sup>PAK**

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 1 of 13</b>
------------------	-----------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### Table of Contents

1.	Introduction	pg. 3
2.	Test vehicles	pg. 4
3.	Failure Criteria	pg. 5
4.	Evaluation plan and results	pg. 6
5.	Appendixes	
	- Technological Characteristics	pg. 9
	- Reliability Test Description	pg. 12



	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### **Introduction**

This report aims at the internal qualification of PSI as new additional assembly location for package D<sup>2</sup>PAK.

The Qualification Reliability test trials have been performed in ST Catania Site.

The evaluation results meet ST products qualification targets, therefore PSI as the new additional assembly location for package D<sup>2</sup>PAK is qualified.

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 3 of 13</b>
------------------	-----------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

**Test Vehicles:**

<b>Product Line</b>	<b>Sales Type</b>	<b>Package</b>
E33E	STB70NF3LL	D <sup>2</sup> PAK
EZ56	STB11NK50Z	D <sup>2</sup> PAK
EZ61	STB3NK60Z	D <sup>2</sup> PAK

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 4 of 13</b>
------------------	-----------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

**Failure Criteria :**

A failed component is a device which becomes inoperative during the test or it fails on meeting the end limits foreseen in the device specification, for one or more than the parameters here below reported

**Power MOSFET Main Parameters**

- Drain Leakage Current ( $I_{dss}$ )
- Gate Leakage Current ( $I_{gss}$ )
- Threshold Voltage ( $V_{gs(th)}$ )
- Forward On Voltage ( $V_{sd}$ )
- Drain Source On Voltage ( $V_{ds(on)}$ )
- Drain Source Breakdown Voltage ( $B_{vds}$ )

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 5 of 13</b>
------------------	-----------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### Reliability Evaluation Plan and results

**D.U.T.: STB70NF3LL**

**Line: E33E**

**Package: D<sup>2</sup>PAK**

<b>Test</b>	<b>Conditions</b>	<b>S.S.</b>	<b>Requirement</b>	<b>Results</b>
<b>PRECONDITIONING OF SMD DEVICES BEFORE TC/THB/ENV. SEQ.</b>	DRYNG 1H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 245°C 3 times	204 x 1 Lot	Parameter deviation within spec. limits at end of preconditioning.	No parameter deviation out of spec. limits at end of preconditioning.
<b>H.T.S.</b>	TA=175°C	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
<b>T.H.B.</b>	D.U.T. SMD PRECONDITIONED TA=85°C - RH=85% Vbias= 24V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
<b>H.T.R.B.</b>	T.A.=175°C Vdd=24V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
<b>H.T.F.B.</b>	TA=150°C Vgss=15V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
<b>PRESSURE POT</b>	TA=121°C - PA=2Atm	77 x 1 Lot	Parameter deviation within spec. limits at 168 hours.	No parameter deviation out of spec. limits at 168 hours.
<b>THERMAL CYCLES AIR TO AIR</b>	D.U.T. SMD PRECONDITIONED TA=-65°C TO 150°C 1 HOUR / CYCLE	77 x 1 Lot	Parameter deviation within spec. limits at 500 cycles.	No parameter deviation out of spec. limits at 500 cy
<b>THERMAL FATIGUE</b>	ΔTC=105°C - Pd=3.8W	77 x 1 Lot	Parameter deviation within spec. limits at 10k cycles.	No parameter deviation out of spec. limits at 10Kcy.
<b>ENVIRONMENTAL SEQUENCE</b>	D.U.T. SMD PRECONDITIONED 100 THERMAL CYCLES + 96H PP	50 x 1 Lot	Parameter deviation within spec. limits at end of test.	No parameter deviation out of spec. limits at end of test.

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 6 of 13</b>
------------------	-------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

## Reliability Evaluation Plan and results

**D.U.T.: STB11NK50Z**

**Line: EZ56**

**Package: D<sup>2</sup>PAK**

<b>Test</b>	<b>Conditions</b>	<b>S.S</b>	<b>Requirement</b>	<b>Results</b>
<b>PRECONDITIONING OF SMD DEVICES BEFORE TC/THB/ENV. SEQ.</b>	DRYNG 1H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 245°C 3 times	204 x 1 Lot	Parameter deviation within spec. limits at end of preconditioning.	No parameter deviation out of spec. limits at end of preconditioning.
<b>H.T.S.</b>	TA=150°C	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>T.H.B.</b>	D.U.T. SMD PRECONDITIONED TA=85°C - RH=85% Vbias = 100V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>H.T.R.B.</b>	T.A.=150°C Vdd=400V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>H.T.F.B.</b>	TA = 150°C Vgss= 30V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>PRESSURE POT</b>	TA=121°C - PA=2Atm	77 x 1 Lot	Parameter deviation within spec. limits at 96 hours.	<i>No parameter deviation out of spec. limits at 96 hours.</i>
<b>THERMAL CYCLES AIR TO AIR</b>	D.U.T. SMD PRECONDITIONED TA=-65°C TO 150°C 1 HOUR / CYCLE	77 x 1 Lot	Parameter deviation within spec. limits at 500 cycles.	<i>No parameter deviation out of spec. limits at 500 cy.</i>
<b>THERMAL FATIGUE</b>	ΔTC=105°C - Pd=3.8W	77 x 1 Lot	Parameter deviation within spec. limits at 10k cycles.	<i>No parameter deviation out of spec. limits at 10 Kcy.</i>
<b>ENVIRONMENTAL SEQUENCE</b>	D.U.T. SMD PRECONDITIONED 100 THERMAL CYCLES + 96H PP	50 x 1 Lot	Parameter deviation within spec. limits at end of test.	<i>No parameter deviation out of spec. limits at end of test.</i>

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 7 of 13</b>
------------------	-------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

## Reliability Evaluation Plan and results

**D.U.T.: STB3NK60Z**

**Line: EZ61**

**Package: D<sup>2</sup>PAK**

<b>Test</b>	<b>Conditions</b>	<b>S.S</b>	<b>Requirement</b>	<b>Results</b>
<b>PRECONDITIONING OF SMD DEVICES BEFORE TC/THB/ENV. SEQ.</b>	DRYNG 1H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 245°C 3 times	204 x 1 Lot	Parameter deviation within spec. limits at end of preconditioning.	No parameter deviation out of spec. limits at end of preconditioning.
<b>H.T.S.</b>	TA=150°C	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>T.H.B.</b>	D.U.T. SMD PRECONDITIONED TA=85°C - RH=85% Vbias = 100V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>H.T.R.B.</b>	T.A.=150°C Vdd=480V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>H.T.F.B.</b>	TA = 150°C Vgss= 30V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	<i>No parameter deviation out of spec. limits at 1000 hours.</i>
<b>PRESSURE POT</b>	TA=121°C - PA=2Atm	77 x 1 Lot	Parameter deviation within spec. limits at 96 hours.	<i>No parameter deviation out of spec. limits at 96 hours.</i>
<b>THERMAL CYCLES AIR TO AIR</b>	D.U.T. SMD PRECONDITIONED TA=-65°C TO 150°C 1 HOUR / CYCLE	77 x 1 Lot	Parameter deviation within spec. limits at 500 cycles.	<i>No parameter deviation out of spec. limits at 500 cy.</i>
<b>THERMAL FATIGUE</b>	ΔTC=105°C - Pd=3.8W	77 x 1 Lot	Parameter deviation within spec. limits at 10k cycles.	<i>No parameter deviation out of spec. limits at 10 Kcy.</i>
<b>ENVIRONMENTAL SEQUENCE</b>	D.U.T. SMD PRECONDITIONED 100 THERMAL CYCLES + 96H PP	50 x 1 Lot	Parameter deviation within spec. limits at end of test.	<i>No parameter deviation out of spec. limits at end of test.</i>

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 8 of 13</b>
------------------	-------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### Technological Characteristics

**D.U.T.: STB70NF3LL**

**Line: E33E**

**Package: D<sup>2</sup>PAK**

<b>DIE</b>	<i>Technology:</i> STripFET II POWER MOSFET <i>Material:</i> Silicon <i>Passivation :</i> No Passivation <i>Metallization – Front :</i> Al/Si (1%) <i>Dimensions :</i> 2540 x 3550 μm <sup>2</sup> <i>- Back :</i> Ti-Ni-Au			
	<b>DIE ATTACH</b>	Soft Solder	<b>FRAME</b>	<i>Frame and lead material:</i> Copper  <i>Frame coating :</i> Raw Copper Ni Spot on T-Post and Leads  <i>Lead coating :</i> Sn
<b>WIRE BOND</b>	Ultrasonics	<b>WIRE</b>	<i>Material :</i> Al Gate Al Source  <i>Diameter :</i> 5 mils Gate 15 mils Source	
<b>SEALING</b>	Molding	<b>PACKAGING</b>	<i>Material :</i>	Epoxy Resin

**PRODUCTION PLACES:**

WAFER PROCESSING: SINGAPORE  
 ASSEMBLY LOCATION : PSI  
 Q.A. LOCATION : PSI

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 9 of 13</b>
------------------	-------------------------------	---------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### Technological Characteristics

**D.U.T.: STB11NK50Z      Line: EZ56      Package: D<sup>2</sup>PAK**

<b>DIE</b>	<i>Technology:</i> SuperMESH™ MOSFET <i>Material:</i> Silicon <i>Passivation :</i> Nitride <i>Metallization – Front :</i> Al/Si (1%) <i>Dimensions :</i> 5040 x 3800 μm <sup>2</sup> <i>- Back :</i> Ti-Ni-Au			
	<b>DIE ATTACH</b>	Soft Solder	<b>FRAME</b>	<i>Frame and lead material:</i> Copper <i>Frame coating :</i> Raw Copper Ni Spot on T-Post and Leads <i>Lead coating :</i> Sn
<b>WIRE BOND</b>	Ultrasonics	<b>WIRE</b>	<i>Material :</i> Al Gate Al Source <i>Diameter :</i> 5 mils Gate 7 mils Source	
<b>SEALING</b>	Molding	<b>PACKAGING</b>	<i>Material :</i>	Epoxy Resin

**PRODUCTION PLACES:**      WAFER PROCESSING: SINGAPORE  
 ASSEMBLY LOCATION : PSI  
 Q.A. LOCATION : PSI

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 10 of 13</b>
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	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### Technological Characteristics

**D.U.T.: STB3NK60Z**

**Line: EZ61**

**Package: D<sup>2</sup>PAK**

<b>DIE</b>	<i>Technology:</i> SuperMESH™ MOSFET			
	<i>Material:</i> Silicon		<i>Passivation</i> : Nitride	
	<i>Metallization – Front :</i> Al/Si (1%)		<i>Dimensions</i> : 2700 x 2170 μm <sup>2</sup>	
	<i>- Back :</i> Ti-Ni-Au			
<b>DIE ATTACH</b>	Soft Solder	<b>FRAME</b>	<i>Frame and lead material:</i>	Copper
			<i>Frame coating :</i>	Raw Copper Ni Spot on T-Post and Leads
			<i>Lead coating :</i>	Sn
<b>WIRE BOND</b>	Ultrasonics	<b>WIRE</b>	<i>Material :</i>	Al Gate Al Source
			<i>Diameter :</i>	5 mils Gate 5 mils Source
<b>SEALING</b>	Molding	<b>PACKAGING</b>	<i>Material :</i>	Epoxy Resin

**PRODUCTION PLACES:**

**WAFER PROCESSING: SINGAPORE**  
**ASSEMBLY LOCATION : PSI**  
**Q.A. LOCATION : PSI**

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 11 of 13</b>
------------------	-----------------------------------	----------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### Reliability Test Description

#### High Temperature Reverse Bias (HTRB )

This test is performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and simultaneously reverse biased. The purpose of this test is to detect surface defects such as poor passivation, presence of contaminants, etc...

#### High Temperature Forward Bias (HTFB)

This test is performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and simultaneously forward gate biased. The purpose of this test is to detect surface and gate oxide defects.

#### High Temperature Storage (HTS)

This stress test is performed to check the device life in a high temperature ambient. Specimens are put for a period of time inside a stove in free air. Detectable failure mechanisms are presence of contaminants and metal corrosion.

#### Thermal Cycles/Shocks

The purpose of this test is to determine the resistance of devices to exposure to extreme changes in temperature. Specimens are first placed in a suitable environment at a low temperature and then transferred to one at high temperature. Effects of thermal cycles/shocks include cracking of die, breaking of wire bonding, mechanical damage to the device case.

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 12 of 13</b>
------------------	-----------------------------------	----------------------

	<b>APM CATANIA RELIABILITY REPORT</b>	<b>Date:</b>	<b>May '07</b>
		<b>No</b>	<b>11/2007</b>

### **Reliability Test Description (continued)**

#### Temperature Humidity Bias (THB)

This test is performed to check the device life in a high humidity ambient. Specimens are subjected to a permanent bias in a climatic chamber in the presence of steam. Detectable failure mechanisms are metal corrosion and moulding defects.

#### Pressure Pot

This test is performed in order to check device life in a high humidity ambient in an accelerated way. Specimens are subjected for a period of time inside an autoclave in the presence of steam and pressure. Detectable failure mechanism is metal corrosion.

#### Thermal Fatigue

This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress). The purpose of this test is to detect assembly defects : improper die-attach, bonding weakness and thermal mismatch among various components of the package.

#### Environmental Sequence

The purpose of this test is to study the influence of corrosion mechanism when the die/package system has already been stressed by temperature cycling.

<b>ISSUED BY</b>	<b>RELIABILITY DEPARTMENT</b>	<b>Page 13 of 13</b>
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