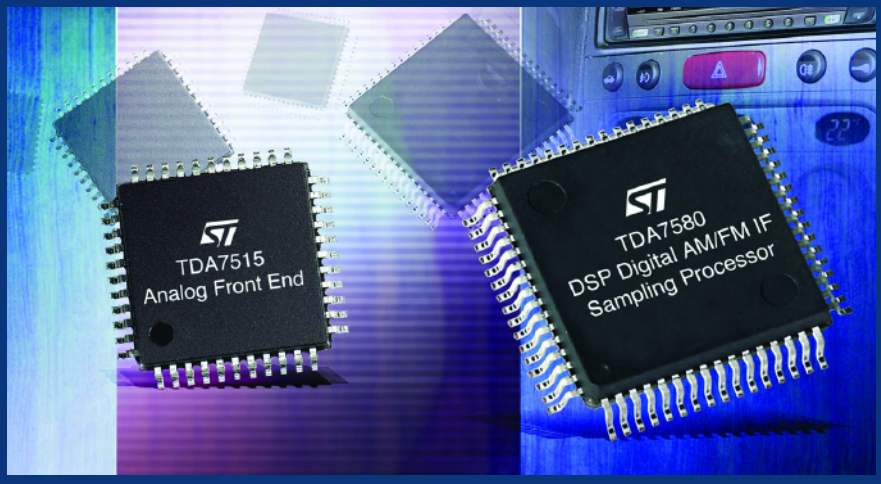
DSP-based AM/FM radio chipset

With IF sampling



STMicroelectronics' TDA7515 and TDA7580 form a DSP-based digital AM/FM radio chipset which directly digitizes intermediate frequencies.

TDA7515

- RF AGC generation by RF and IF detection
- I/Q mixer for FM IF 10.7MHz with image rejection and programmable IF tank adjust for FM and AM
- Preamplifier and mixer for IF 10.7MHz AM upconversion
- VCO and programmable divider for "world receiver"
- Programmable, low noise IF amplifier with integrated AGC
- High-performance fast PLL for RDS-system
- Electronic alignment for preselection stages
- All functions bus-controlled

TDA7580

- FM/AM IF sampling DSP
- On-chip analogue to digital converter for 10.7MHz IF signal conversion
- Software based channel equalization
- FM adjacent channel suppression
- Reception enhancement in multipath condition
- Stereo decoder and weak signal processing
- 2-channel serial audio interface (SAI) with sample rate converter
- I^2C and buffer-SPI controlled interface
- RDS filter, demodulator and decoder
- Inter-processor transport interface for antenna and tuner diversity
- Front-end AGC feedback

TDA7580 Digital IF sampling processor

The TDA7580 is an IC which implements an advanced mixed analogue and digital solution to perform signal processing of an AM/FM channel. The chip has been designed to perform digital equalization of the FM/AM channel and real rejection of adjacent channels, as well as any other interference with the selected signal. In severe multiple path conditions, reception is improved to deliver high-quality audio. The algorithm is self-adaptive, thus requiring no "in-the-field" adjustments after parameter optimization.

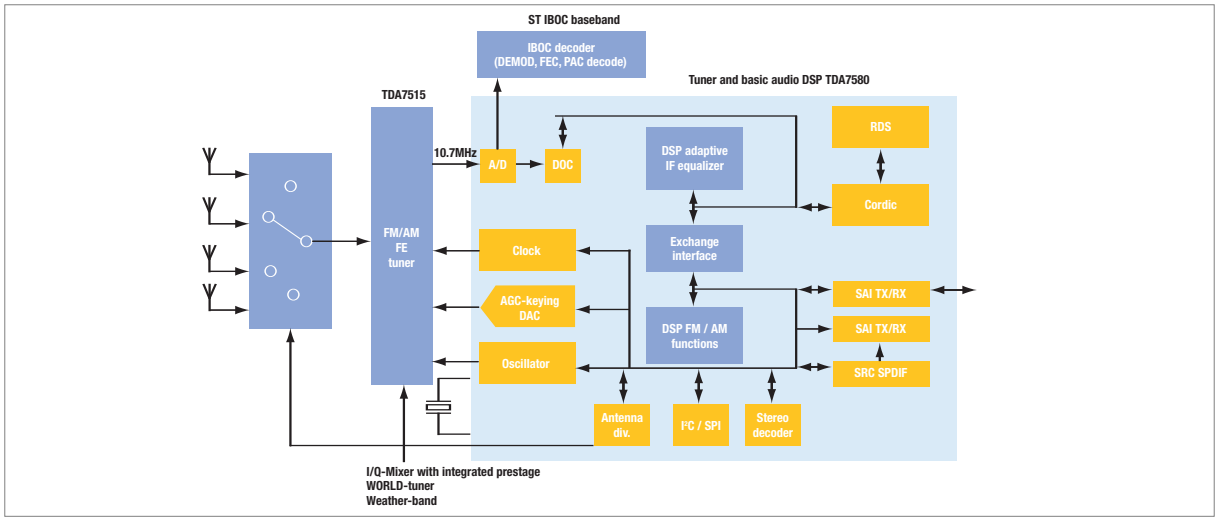
The TDA7580 has a built-in band-pass sigma delta A/D converter for 10.7MHz IF conversion from the TDA7515. The 24bit-DSP allows flexibility of algorithm implementation, thus giving some freedom for customer-specific features. The processing power offers significant headroom for a customer's software requirement, even when the channel equalization and decoding software is running. Program and data memory space can be loaded from an external non-volatile memory via I²C or SPI.

The oscillator module works with an external 74.1MHz quartz crystal. It has very low EMI, it introduces very low distortion and harmonics fall outside the radio bandwidth. The companion tuner device receives reference timing through a differential ended interface, supplied by the oscillator module which accurately divides down the master clock frequency. After IF conversion, the digitized baseband signal passes through the baseband processing section, either FM or AM, depending on listener choice. FM baseband processing comprises stereo decoder, spike detection and noise blanking. AM noise blanking is implemented fully in software.

The internal RDS filter, demodulator and decoder features complete functions, so that output data is available through either an I²C or SPI interface. No DSP support is needed, except at start-up, so that RDS can work in the background and in parallel with other DSP processing. This mode (RDS-only) offers lower current consumption for low-power application modes. An I²C/SPI interface is available for control and communication with the main micro, as well as the RDS data interface. The DSP SPI block embeds a 10-word FIFO for both transmit and receive channels, to reduce the DSP task and allow frequent response to the interrupt from the control interface.

Serial audio interface (SAI) is the ideal solution for audio data transfer, both transmit and receive, either master or slave. The flexibility of this module gives a wide choice of different protocols, including I²S. Two fully independent bidirectional data channels, with separate clocks, allow the use of the TDA7580 as a general-purpose digital audio processor.

A fully asynchronous sample rate converter (ASRC) can be used prior to sending audio data out via the SAI, so that the internal audio sampling rate can be adapted by up-conversion to any external rate. An inter-processor transport interface (HS3I, high speed synchronous serial interface) is also available for modular systems which implement dual tuner diversity, thus enhancing overall system performance. General purpose I/O registers are connected to, and controlled by, the DSP by means of a memory map. A debug and test interface is available for on-chip software debug as well as for internal register read/write operations.



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