# VND5004ASP30-E (VH01)

# Package MultiPowerSO30
# New frame for sagging wire improvement

| Revision history | | | |
|---|---|---|---|
| **Rev.** | **Date of Release** | **Author** | **Changes description** |
| 0.1 | September 4th 2014 | F. Ceraulo - APG Q&R Catania | Creation |

## Table of contents

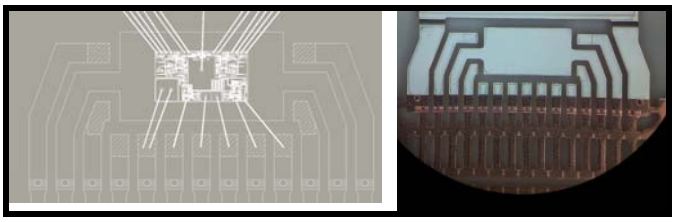
# - 1. Reliability evaluations overview

## 1.1 Objectives

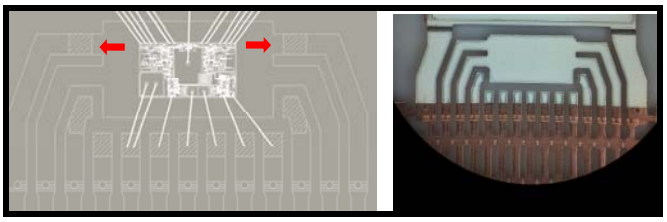
Aim of this report is to present the results of the reliability evaluations performed on **VND5004ASP30-E** (VH01 as ST internal code) chosen as test vehicle to release in production a new frame for package MultiPowerSO30.

This product is a 4mohm Dual Channel High Side Driver with analog current sense for Automotive Applications designed in VIPower M05 technology, composed by two power dice (VNI4 as ST internal silicon line) and one signal die (VNG4 as ST internal silicon line) both diffused in ST AMK6 Ang Mo Kio (Singapore) 6" wafer fab.

The new frame is introduced for sagging wire improvement and was designed to make the floating paddle more rigid reducing the vertical vibration during handling.



**Current frame**



**New frame**

Change between the current and the new frames occurs only in a geometry dimension (see red arrows for details) but not in the material or in the assembly configuration.

The qualification was done according to **AEC_Q100 Rev.G** specification following the path described here below:

| Test group as per **AEC-Q100 Rev.G** | | Performed (Y/N) | Comment |
|---|---|---|---|
| A | Accelerated Environment Stress | Y | |
| B | Accelerated Lifetime Simulation | N | Not applicable |
| C | Package Assembly Integrity | Y | |
| D | Die Fabrication Reliability | N | Not applicable |
| E | Electrical Verification | N | Not applicable |
| F | Defect Screening | N | Not applicable |
| G | Cavity Package Integrity | N | N/A: not for plastic packaged devices |

See details per each test group in section 4 of this report.

In the below table a comparison between the AEC-Q100 and ZVEI requirements for this kind of change (lead frame dimension) vs the applied ST qualification plan is reported:

| | Test Group A | | | | | Test Group B | | Test Group C | | | | Test Group D | | | | | Test Group E | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | THB | AC | TC | PTC | HTSL | HTOL | ELFR | WBS | WBP | SD | PD | EM | TDDB | HCI | NBTI | SM | HBM | CDM | LU | ED | GL | EMC | SC |
| AEC-Q100 | | x | x | x | | | | | | x | x | | | | | | | | | | | | x |
| ZVEI | | x | x | x | | | | | | x | x | | | | | | | | | | | | x |
| ST | | x | x | | | | | x | x | x | x | | | | | | | | | | | | |

The applied qualification plan was addressed to investigate about failure mechanisms related to the thermo mechanical and humidity stress while the impact of the change is considered negligible vs the failure mechanism related to PTC and SC (no change in wires/assembly configuration/die attach).

### 1.2 Results

All reliability tests have been completed with positive results neither functional nor parametric rejects were detected at final electrical testing.

The Package Assembly Integrity (test Group C) pointed out neither abnormal break loads nor forbidden failure modes.

**Based on the overall positive results we consider the products qualified from a reliability point of view.**

# - 2. Traceability

| Wafer fab information | |
|---|---|
| **Wafer fab manufacturing location** | ST AMK6 Ang Mo Kio (Singapore) |
| **Wafer diameter (inches)** | 6 |
| **Silicon process technology** | VIPower M05 |
| **Die finishing back side** | Ti-Ni-Au |
| **Die size (micron)** | VNG4 (signal): 2800 x 1560<br>VNI4 (power) : 7990 x 4000 |
| **Metal levels / materials** | VNG4 (signal): 2 levels / Ti/TiN/Ti/AlSiCu (3.2 µm last level)<br>VNI4 (power) : 1 level / Ti/AlSiCu (4.5 µm) |
| **Die finishing front side** | SiN/POLYIMIDE |
| **Diffusion Lots #** | VNG4 (signal): 61431X3, VNI4 (power): 63245T5 |

| Assembly Information | |
|---|---|
| **Assembly plant location** | ST Muar (Malaysia) |
| **Package description** | Multi PowerSO_30 |
| **Molding compound** | RESIN SUMITOMO EME-G600C |
| **Wires bonding materials/diameters** | Au 1.2mils (on signal) / Al 15mils (on power) |
| **Die attach material** | GLUE QMI9507<br>PREFORM Pb/Ag/Sn 97.5/1.5/1 |
| **Assembly Lots #** | 993360NR01 (old frame), 993360NR02 (new frame) |

| Reliability Information | |
|---|---|
| **Reliability test execution location** | ST Catania (Italy) |

# - 3. Device characteristics

## 3.1 Generalities

# VND5004A-E
# VND5004ASP30-E

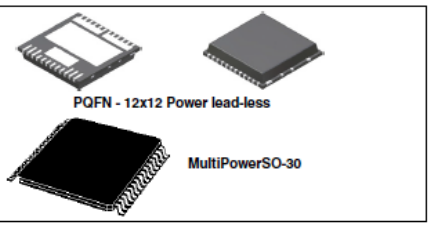
Double 4mΩ high side driver with analog current sense for automotive applications

### Features

| | | |
|---|---|---|
| Max transient supply voltage | $V_{CC}$ | 41V |
| Operating voltage range | $V_{CC}$ | 4.5 to 27V |
| Max On-State resistance (per ch.) | $R_{ON}$ | 4 mΩ |
| Current limitation (typ) | $I_{LIMH}$ | 100A |
| Off state supply current | $I_S$ | 2 µA(1) |

1. Typical value with all loads connected

- General
  - Inrush current active management by power limitation
  - Very low stand-by current
  - 3.0V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC European directive
- Diagnostic functions
  - Proportional load current sense
  - Current sense disable
  - Thermal shutdown indication
- Protection
  - Undervoltage shut-down
  - Overvoltage clamp
  - Load current limitation
  - Thermal shut down
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of $V_{CC}$
  - Reverse battery protection with self switch on of the PowerMOS (see *Application schematic on page 18*)
  - Electrostatic discharge protection




### Application

- All types of resistive, inductive and capacitive loads
- Suitable for power management applications

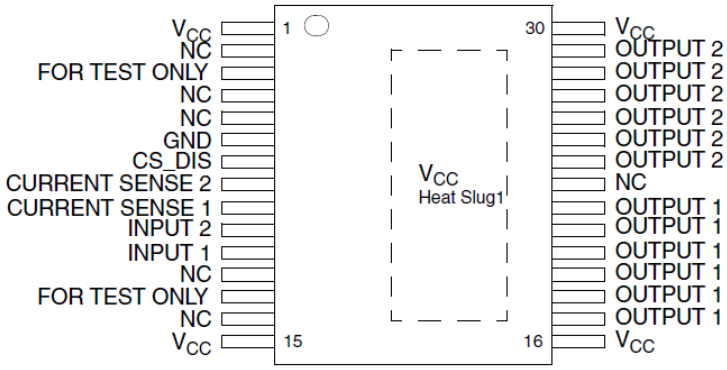
### Description

The VND5004ATR-E and VND5004ASP30-E are devices made using STMicroelectronics VIPower technology. They are intended for driving resistive or inductive loads with one side connected to ground. Active $V_{CC}$ pin voltage clamp and load dump protection circuit protect the devices against transients on the Vcc pin (see ISO7637 transient compatibility table). These devices integrate an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is high impedance. Output current limitation protects the devices in overload condition. In case of long duration overload, the devicesa limit the dissipated power to a safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as a fault condition disappears.

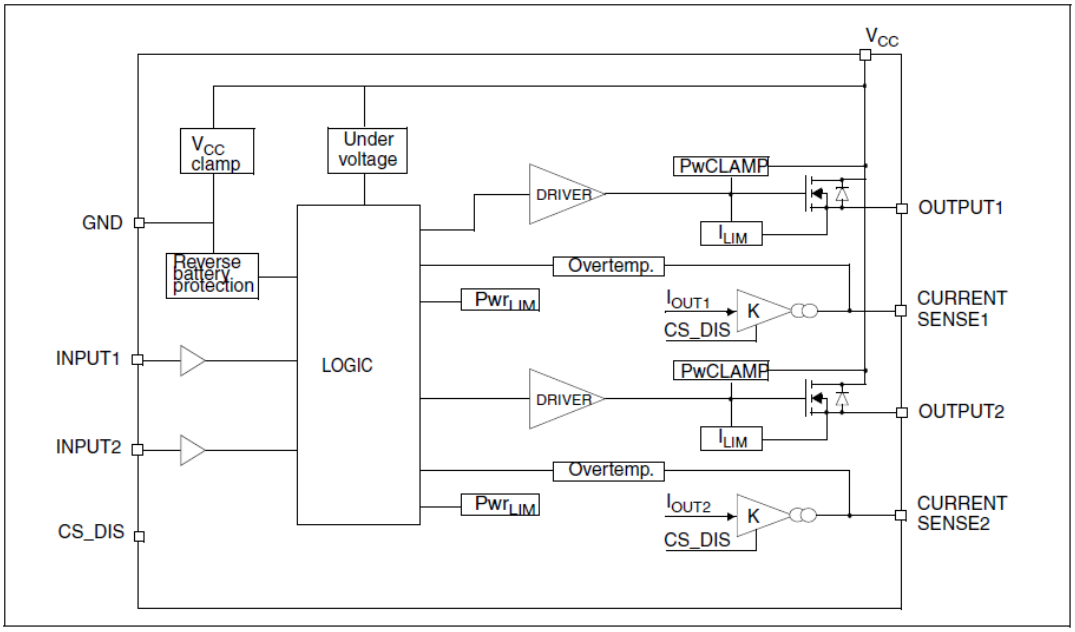
**Table 1. Devices summary**

| Package | Order codes | | |
|---|---|---|---|
| | Tube | Tape and Reel | Tray |
| PQFN-12x12 Power lead-less | - | VND5004ATR-E | VND5004A-E |
| MultiPowerSO-30 | VND5004ASP30-E | VND5004ASP30TR-E | - |

## 3.2 Pins connection




## 3.3 Blocks diagram



# - 4. Reliability qualification plan and results

| Test group A: Accelerated Environment Stress | | | | | |
|---|---|---|---|---|---|
| **AEC #** | **Test Name** | **STM Test Conditions** | **Sample Size/ Lots** | **Results Fails/SS/Lots** | **Comments** |
| **A1** | **PC**<br>Pre Cond | - Preconditioning according to Jedec JESD22-A113F including 5 Temperature Cycling Ta=-40ºC/+60ºC<br>- Reflow according to level 3 Jedec JSTD020D-1<br>- 100 Temperature Cycling Ta=-50ºC/+150ºC | Before AC, TC | | |
| **A2** | **THB**<br>Temp Humidity Bias | Ta=85ºC, RH=85%, Vcc=24V for 1000 hours | - | - | Not Applicable |
| **A3** | **AC**<br>Autoclave | **ENV. SEQ.** Enviromental Sequence<br><br>**TC** (Ta=-65ºC / +150ºC for 100 cycles) +<br>**AC** (Ta=121ºC, Pa=2atm for 96 hours) | 77/2 | 0/77/2 | 1 Lot old frame<br>1 Lot new frame |
| **A4** | **TC**<br>Temp. Cycling | Ta=-65ºC / +150ºC for 500 cycles | 77/2 | 0/77/2 | 1 Lot old frame<br>1 Lot new frame |
| **A5** | **PTC**<br>Power Temp. Cycling | Ta=-40ºC / +125ºC for 1000 cycles. | - | - | Not Applicable |
| **A6** | **HTSL**<br>High Temp. Storage Life | Ta=150ºC for 1000 hours. | - | - | Not Applicable |

| Test group A: Accelerated Environment Stress Robustness activity | | | | | |
|---|---|---|---|---|---|
| **AEC #** | **Test Name** | **STM Test Conditions** | **Sample Size/ Lots** | **Results Fails/SS/Lots** | **Comments** |
| **A4** | **TC**<br>Temp. Cycling | Ta=-50ºC / +150ºC **for 1000 cycles** | 77/2 | 0/77/2 | 1 Lot old frame<br>1 Lot new frame |

| Test group B: Accelerated Lifetime Simulation | | | | | |
|---|---|---|---|---|---|
| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
| B1 | **HTOL** High Temp. Op. Life | Bias Static stress (JESD22-A108): **HTB** Tamb=125ºC, Vcc=28V for 1000 hours | - | - | Not Applicable |
| B2 | **ELFR** Early Life Failure Rate | Parts submitted to **HTOL** per JESD22-A108 requirements; GRADE 1: 24 hours at 150ºC | - | - | Not Applicable |
| B3 | **EDR** Endurance Data Retention | Only for memory devices | - | - | Not Applicable |

| Test group C: Package Assembly Integrity | | | | | |
|---|---|---|---|---|---|
| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
| C1 | **WBS** Wire Bond Shear | | 30 bonds /minimum 5 units/1 lot | All measurement within spec limits | 1 Lot old frame<br>1 Lot new frame |
| C2 | **WBP** Wire Bond Pull | | 30 bonds /minimum 5 units/1 lot | All measurement within spec limits | 1 Lot old frame<br>1 Lot new frame |
| C3 | **SD** Solderability | | 15/4 | Passed | 1 Lot old frame<br>1 Lot new frame |
| C4 | **PD** Physical Dimensions | | 10/4 | Passed | 1 Lot old frame<br>1 Lot new frame |
| C5 | **SBS** Solder Ball Shear | Only for BGA package | - | - | Not Applicable |
| C6 | **LI** Lead Integrity | Not required for Surface Mount Devices | - | - | Not Applicable |

| Test group D: Die Fabrication Reliability | | | | | |
|---|---|---|---|---|---|
| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
| D1 | **EM** Electromigration | | - | - | Not Applicable |
| D2 | **TDDB** Time Dependent Dielectric Breakdown | | - | - | Not Applicable |
| D3 | **HCI** Hot Carrier Injection | | - | - | Not Applicable |
| D4 | **NBTI** Negative Bias Temperature Instability | | - | - | Not Applicable |
| D5 | **SM** Stress Migration | | - | - | Not Applicable |

| Test group E: Electrical Verification | | | | | |
|---|---|---|---|---|---|
| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
| E2 | **ESD** HBM / MM | | - | - | Not Applicable |
| E3 | **ESD** CDM | | - | - | Not Applicable |
| E4 | **LU** Latch-Up | | - | - | Not Applicable |
| E5 | **ED** Electrical Distributions | | - | - | Not Applicable |
| E7 | **CHAR** Characterization | | - | - | Not Applicable |
| E8 | **GL** Gate Leakage | | - | - | Not Applicable |
| E9 | **EMC** Electromagnetic Compatibility | | - | - | Not Applicable |

| | | | | |
|---|---|---|---|---|
| **E10** | **SC**<br>Short Circuit Characterization | According to **AEC-Q100-012** | - | Not Applicable |

| Test group F: Defects Screening Tests | | | | | |
|---|---|---|---|---|---|
| **AEC #** | **Test Name** | **STM Test Conditions** | **Sample Size/ Lots** | **Results Fails/SS/Lots** | **Comments** |
| **F1** | **PAT**<br>Process Average Testing | | Not Applicable | | |
| **F2** | **SBA**<br>Statistical Bin/Yield Analysis | | | | |

| Test group G: Cavity Package Integrity Tests | | | | | |
|---|---|---|---|---|---|
| **AEC #** | **Test Name** | **STM Test Conditions** | **Sample Size/ Lots** | **Results Fails/SS/Lots** | **Comments** |
| **G1** | **MS**<br>Mechanical Shock | Not applicable: not for plastic packaged devices | | | |
| **G2** | **VFV**<br>Variable Frequency Vibration | | | | |
| **G3** | **CA**<br>Constant Acceleration | | | | |
| **G4** | **GFL**<br>Gross/Fine Leak | | | | |
| **G5** | **DROP**<br>Package Drop | | | | |
| **G6** | **LT**<br>Lid Torque | | | | |
| **G7** | **DS**<br>Die Shear | | | | |
| **G8** | **IWV**<br>Internal Water Vapor | | | | |

# VIPower housed in PowerSO-30: Wire Sagging Improvement



**WHAT:**
In order to improve quality a modification of lead frame has been implemented. Corner leads are fused together in order to improve wire sagging and to avoid pad tilt/movement during handling

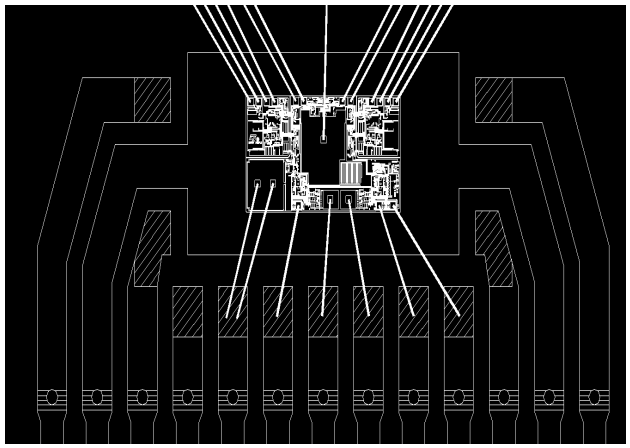
**WHY:**
Quality Improvement

**HOW:**
See enclosed description of the change and qualification report RR002714CT2235

**HOW:**
Change will be implemented according the following schedule
Samples: Available on demand
Qualification results: enclosed to this communication
Implementation: May 2015, but we are ready to implement the change prior this date upon Customer agreement

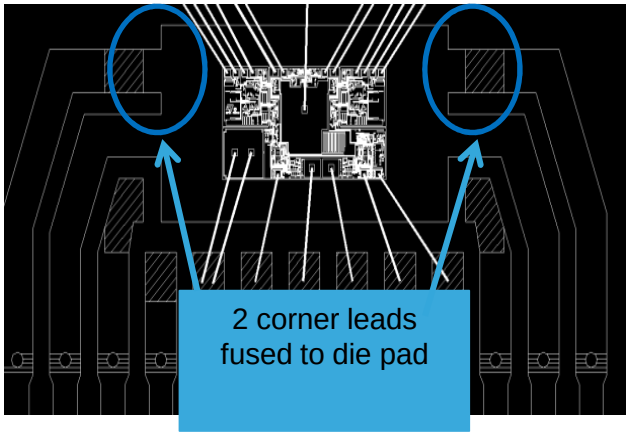
# VIPower housed in PowerSO-30: Wire Sagging Improvement

**Current**



No corner leads are fused together in

**New**




Corner leads are fused together in order to improve wire sagging and to avoid pad tilt/movement during handling

life.augmented