Reliability Report

Qualification of a New Subcontractor for SO16 Package

Package: SO16 - Amkor
T.V: ULQ2003D1013TR

General Information	
Product Line	L203
Product Description	Multidarlington Array
P/N	ULQ2003D1013TR
Product Group	IPD
Product division	IND.& POWER CONV Voltage Regulator & Vre
Packages	SO16
Silicon Process technology	Bipolar

Locations	
Wafer fab	*Ang Mo kio*
Assembly plant	AMKOR
Reliability Lab	*Catania Reliability LAB*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	August 2015	6	Angelo Basile	Giovanni Presti	Final Report

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
STD	Standard

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

SO16 Qualification in AMKOR subcontractor
T.V.:Darlington Arrays ULQ2003D1013TR

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The ULQ2001A, ULQ2002A, ULQ2003 and ULQ2004A are high voltage, high current Darlington arrays each containing seven open collector Darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout

4.2 Construction note

P/N	ULQ2003D1013TR
Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio SINGAPORE
Technology	BiP > 6um
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	2280, 1200 micron
Passivation type	SiN (nitride)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ASL1000
Test program	CL203CB6_0300.zip
Assembly information	
Assembly site	AMKOR ATP1
Package description	SO 16
Molding compound	Epoxy
Die attach material	Glue
Wires bonding materials/diameters	Cu - 1.0mil
Final testing information	
Testing location	AMKOR ATP3
Tester	ASL 1000
Test program	L203_STS_FA 02.prg /l203 STS QAprg_

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Trace Code	Package	Line	Comment
1 Lot	MBQ7*L203DA6	SO16L	L20303	STD
2 lot				STD
3 lot				STD
4 lot				Corner lot HH
5 lot				Corner lot LL

5.2 Test plan and results summary

P/N: ULQ2003D1013TR

Test	PC	Std ref.	Conditions	SS	Steps h=hours cy=cycles	Failure/SS					Note
						1 Lot	2 Lot	3 Lot	Lot HH	Lot LL	
Die Oriented Tests											
HTOL	N	JESD22 A-108	Ta =125°C Vbias+50V		168h	0/77	0/77	0/77			
					500h	0/77	0/77	0/77			
					1000h	0/77	0/77	0/77			
HTSL	N	JESD22 A-103	Ta = 150°C		168h	0/45	0/45	0/45	0/45	0/45	
					500h	0/45	0/45	0/45	0/45	0/45	
					1000h	0/45	0/45	0/45	0/45	0/45	
HTSL	N	JESD22 A-103	Ta = 175°C		168h	0/45	0/45	0/45			Engineering evaluation
					500h	0/45	0/45	0/45			
					1000h	0/45	0/45	0/45			
Package Oriented Tests											
PC	Y	JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168h	0/77	0/77	0/77			
THB	Y	JESD22 A-101	Ta = 85°C, Rh=85% Vbias +35V		168h	0/77	0/77	0/77			
					500h	0/77	0/77	0/77			
					1000h	0/77	0/77	0/77			
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy	0/77	0/77	0/77	0/77	0/77	
					300cy	0/77	0/77	0/77	0/77	0/77	
					500cy	0/77	0/77	0/77	0/77	0/77	

6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.