Reliability Evaluation Report

MDG-MCD-RER1804

F9GO2S Technology Rousset

BEOL Aluminum to Copper

(PCN10962- PCN13039- PCN12921- PCN12922)

General Information	
Commercial Product for test vehicle:	STM32L073VZT6 STM32L083CZT6 STM32L072RZI6 STM32L071KBU6 STM32L072CZY6TR STM32L072RZI6DTR STM32L071RBH6
Product Line:	447X66
Die revision:	X447CCCQ - X447CCCP
Product Description:	STM32L
Package:	LQFP100 14x14x1.4 LQFP64 10x10x1.4 LQFP32/48 7x7x1.4 UFBGA64 5x5x0.6 UFBGA100 7x7x0.6 UFQFPN32 5x5x0.55 WLCSP49 TFBGA64 5x5x1.2
Silicon Technology:	CMOSF9S Rousset
Division:	MDG-MCD

Traceability	
Diffusion Plant:	*Rousset R8*
Assembly Plant:	*ST Muar (Malaysia)* *ASE (Taiwan)* *JSCC (China)* *SCS (Singapore)* *AMKOR (Philippines)*
Reliability Assessment	
Pass	☒
Fail	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	14th September 2020	Céline Navarro	MDG-MCD-QA Back end

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Function	Location	Name	Date
FE Quality Manager	ST Rousset	Antonio DI-GIACOMO	14th September 2020
BE Quality Manager	ST Rousset	Gisèle SEUBE	14th September 2020
Division Quality Manager	ST Rousset	Pascal NARCHE	14th September 2020

Version	Date	Author	Function
2.0	29th September 2021	Cédric CHASTANG	MDG-MCD-QA Back end

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Version	Date	Author	Function
3.0	24th January 2022	Céline NAVARRO	MDG-MCD-QA Back end

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation performed for the following products diffused in ST Rousset (CMOSF9GO2S 110 nm) with full Cu process Back End of the Line (BEOL) and assembled in the listed packages:

Test vehicle is described here below:

Product	Package	Diffusion or Assembly plant
STM32L073VZT6	LQFP100 14x14x1.4	ST Muar (Malaysia)
STM32L083CZT6	LQFP48 7x7x1.4 (1)	JSCC (China)
STM32L072RZI6	UFBGA64 5x5x0.6 (2)	ASE KH (Taiwan)
STM32L071KBU6	UFQFPN32 5x5x0.55	JSCC (China)
STM32L072CZY6TR	WLCSP49	ASE KH (Taiwan)
STM32L072CZY6TR	WLCSP49	SCS (Singapore)
STM32L072RZI6DTR	UFBGA64 5x5x0.6	AMKOR (Philippine)
STM32L071RBH6	TFBGA64 5x5x1.2	ST Muar (Malaysia)

(1) Similarity applied for LQFP32/64 at JSCC as test vehicle in LQFP48 assembled in same production line.
(2) Similarity applied for UFBGA100 7x7x0.6 at ASE as test vehicle in UFBGA64 5x5x0.6 assembled in same production line.

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

This Production Change Notification (PCN) concerns process brick (process step) from wafer fabrication to Rousset 8''.

For PCN10962 & PCN13039, Changes are described here below:

	Old:	New:
Description	Aluminum interconnect back end of line in Rousset 8".	Copper interconnect back end of line in Rousset 8"

For PCN 12921, changes are described here below:

	UFBGA5x5 Assembly Lines					
	Current lines					Added line
Back-End Site	ASE Kaohsiung	AMKOR ATP	ASE Kaohsiung	AMKOR ATP	ASE Kaohsiung	AMKOR ATP
Product line Diffusion process variant	Crolles BEOL Copper		Rousset BEOL Aluminium		Rousset BEOL Copper	

For PCN 12922, changes are described here below:

	ST MUAR Back-End Site TFBGA5x5 Assembly Lines			
	Current lines			Added line
Product line Diffusion process variant	Crolles BEOL Copper	Rousset BEOL Aluminium		Rousset BEOL Copper

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for all Finished Goods diffused in ST Rousset 8'' CMOSF9GO2S 110nm and assembled in the following packages: LQFP100 14x14 Muar, LQFP48 7x7 JSCC, UFBGA5x5 ASE, UQFN32 5x5 JSCC, WLSCP49 ASE and SCS, UFBGA5x5 AMKOR.

For TFBGA5x5 MUAR, final results are expected early of March2022.

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

STM32 Die Test Vehicles

Package line	Assembly Line Package	Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
LQFP	ST MUAR	LQFP 14X14 100L	447 / 1L*447	R8 Rousset	3
	JSCC	LQFP 10X10 64L	417 / 5W*417	R8 Rousset	1

STM32 Package Test Vehicles

Package line	Assembly Line Package	Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
LQFP	ST MUAR	LQFP 14X14 100L	447 / 1L*447	R8 Rousset	3
	JSCC	LQFP 10X10 64L	417 / 5W*417	R8 Rousset	1
	JSCC	LQFP 7X7 48L	447 / 5B*447	R8 Rousset	1
QFN	JSCC	UFQFPN 5X5 32L	447 / MG*447	R8 Rousset	1
WLCSP	SCS	WLCSP 49L	447 / 51*447	R8 Rousset	1
WLCSP	ASE KH	WLCSP 49L	447 / 51*447	R8 Rousset	1
UFBGA	ASE KH	UFBGA64 5x5x0.6	447 / 21*447	R8 Rousset	1
UFBGA	AMKOR	UFBGA64 5x5x0.6	447 / 21*447	R8 Rousset	1
TFBGA	MUAR	TFBGA64 5x5x1.2	447 / R8*447	R8 Rousset	1

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1 die 447	
Wafer fab name / location	R8 ST Rousset
Wafer diameter (inches)	8
Wafer thickness (µm)	725+/-25 µm
Silicon process technology	CMOSF9S
Number of masks	37
Die finishing front side (passivation) materials	USG + NitUV (HFP USG+UV Nitride)
Die finishing back side Materials	RAW SILICON - BACK GRINDING
Die area (Stepping die size)	3329,3293 µm
Die pad size	53,108 µm
Sawing street width (X,Y) (µm)	80,80 µm
Metal levels/Materials/Thicknesses	Metal 1 TaN/Ta/Cu 0.260 Metal 2 TaN/Ta/Cu 0.360 µm Metal 3 TaN/Ta/Cu 0.360 µm Metal 4 TaN/Ta/Cu 0.360 µm Metal 5 Ti/AlCu/TxTN 1.200 µm

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 - LQFP14X14 100L	
Assembly plant name / location	ST MUAR (Malaysia)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	381 µm +/- 25µm
Die sawing method	Step cut
Bill of Material elements	
Lead frame	FRAME LQFP 100L 14SQ 5.2sqOpB RgAg+CuOx
Lead frame finishing (material/thickness)	Pure Tin (e3) Tolerance 7 to 20µm
Die attach material/type glue/supplier	ABLESTIK ABP8302
Wire bonding material/diameter	WIRE Ag 96.5% D0.8
Molding compound material/supplier/reference	SUMITOMO EME-G700LS
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3
Package 3 - LQFP7x7 48L	
Assembly plant name / location	JSCC (China)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 µm +/- 25µm
Die sawing method	Step cut
Bill of Material elements	
Lead frame	LQFP48L 210sq no slots STMP LF JSCC
Lead frame finishing (material/thickness)	Pure Tin (e3) Tolerance 7 to 20µm
Die attach material/type glue/supplier	Ablestik 3230
Wire bonding material/diameter	Ag 96.5 0.8 MIL Diam
Molding compound material/supplier/reference	Sumitomo low alpha G631SHQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 4 - UFBGA5x5 64L	
Assembly plant name / location	ASE (Taiwan)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75 µm +/- 12µm
Die sawing method	Step cut
Bill of Material elements	
Substrate (BGA)	UFBGA 5x5 64L P0.5
Balls metallurgy/diameter (BGA)	200 DIAM SN96.5 AG3.5%
Die attach material/type film/supplier	D/A Tape ABLESTICK ATB-125
Wire bonding material/diameter	wire gold 0.8 mils
Molding compound material/supplier/reference	KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

Package 5 - UFQFPN5x5 32L	
Assembly plant name / location	JSCC (China)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 µm +/- 25µm
Die sawing method	Step cut
Bill of Material elements	
Lead frame	UQFN 5x5 32L
Lead frame finishing (material/thickness)	Pure Tin (e3) Tolerance 7 to 20µm
Die attach material/type glue/supplier	ABLEBOND 8290
Wire bonding material/diameter	Ag 96.5 0.8 MIL Diam
Molding compound material/supplier/reference	SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 6 - WLCSP49L	
Assembly plant name / location	ASE (Taiwan)
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	355 +/- 25µm
Die sawing method	Mechanical sawing + Step cut
Bill of Material elements	
Balls metallurgy/diameter (CSP)	Solder balls SAC 405 Diam 230µm
Routing/Redistribution layer (RDL) material (CSP)	RDL Copper 8.3um
PBO passivation material (CSP)	Polymide passivation - HD 4100 - R010-0006X
Backside coating material (CSP)	Back side coating PET film
Package Moisture Sensitivity Level (JEDEC J-STD020D)	1
Package 7 - WLCSP49L	
Assembly plant name / location	SCS (Singapore)
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	355 +/- 25µm
Die sawing method	Mechanical sawing + Step cut
Bill of Material elements	
Balls metallurgy/diameter (CSP)	Solder balls SACN 125 Diam 230µm
Routing/Redistribution layer (RDL) material (CSP)	RDL Copper
PBO passivation material (CSP)	Polymide passivation - HD 4100 - R010-0006X
Backside coating material (CSP)	Back side coating PET film
Package Moisture Sensitivity Level (JEDEC J-STD020D)	1

Package 8 - UFBGA 64L AMKOR	
Assembly plant name / location	AMKOR (Philippines)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75 +/- 12µm
Die sawing method	Step cut
Bill of Material elements	
Substrate (BGA)	UFBGA 5x5 64L P0.5
Balls metallurgy/diameter (BGA)	200 DIAM SN96.5 AG3.5%
Die attach material/type film/supplier	DAF Ablestik ATB130U
Wire bonding material/diameter	wire gold 0.8 mils
Molding compound material/reference	GE100LFCS
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 9 - TFBGA 64L MUAR	
Assembly plant name / location	ST MUAR
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	250 +/- 25µm
Die sawing method	Step cut
Bill of Material elements	
Substrate (BGA)	TFBGA5x5 64L P0.5
Balls metallurgy/diameter (BGA)	SACN125 D0.30mm
Die attach material/type film/supplier	ABLESTIK 2100A
Wire bonding material/diameter	wire gold 0.8 mils
Molding compound material/reference	GE-100LF1-2
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	ST RSST in Rousset
	ATP AMKOR in Philippine
	ST Muar (Malaysia

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Assembly Line Package
1	VG821858	Cut 2.1	998320XP	U01L*447ISCQ	LQFP14x14 100L	MUAR
2	VG804754R	Cut 2.1	998321FL(R)	U01L*447ISCQ	LQFP14x14 100L	MUAR
3	VG804754X	Cut 2.1	998321FL(Q)	U01L*447ISCQ	LQFP14x14 100L	MUAR
5	VG821858	Cut 2.1	GQ84823L	S05B*447ESCQ	LQFP7x7 48L	JSCC
6	VG804754	Cut 2.1	AA904046	E12I*447ESCQ	UFBGA5x5 64L	ASE KH
7	VG804754	Cut 2.1	GQ84824R	S4MG*447ESCQ	UFQFPN 5x5 32L	JSCC
8	VG752527	Cut 2.1	AA849073	E151*447ESCQ	WLCSP49L	ASE KH
9	VG821858	Cut 2.1	8N848XZ6	H151*447ESCQ	WLCSP49L	SCS
10	VG048626	Cut 2.1	7B126A5J	P02I*447ESCP	UFBGA5x5 64L	ATP
11	VG048626	Cut 2.1	991360Q8	U3R8*447ESCP	TFBGA5x5 64L	MUAR

3.2 Test plan and results summary

Table 5 - ACCELERATED LIFETIME SIMULATION TESTS

447 LQFP14x14 100L, MUAR

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 1200H 3V6	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 447: 1kV (class 1C)	3	3	9	Lot 1: 0/3 Lot 2: 0/3 Lot 3: 0/3	
LatchUp	JESD78	130°C, 100mA	3	6	18	Lot 1: 0/6 Lot 2: 0/6 Lot 3: 0/6	
EDR	JESD22-A117	A0/R1 10kcy E^2P 100kcy E^2D +1500h @ 105°C then Storage	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
EDR	JESD22-A117	A0/R1 10kcy E^2P 100kcy E^2D +168h @ 25°C then Storage	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
EDR	JESD22-A117	A0/R1 10kcy E^2P 100kcy E^2D +168h @ -40°C then Storage	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
ELFR	JESD22-A108 JESD74	Ta=125°C Duration= 48hrs 3V6	3	800	2400	Lot 1: 0/800 Lot 2: 0/800 Lot 3: 0/800	

Table 6 – ACCELERATED ENVIRONMENT STRESS TESTS

447 LQFP14x14 100L, MUAR

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	250V	3	3	9	Lot 1: 0/3 Lot 2: 0/3 Lot 3: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3	308	924	Lot 1: 0/308 Lot 2: 0/308 Lot 3: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

447 LQFP7x7 48L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	500V	1	3	3	Lot 5: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 5: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 5: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 5: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 5: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 5: 0/77	

447 UFBGA5x5 64L, ASE KH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	500V	1	3	3	Lot 6: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 6: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 6: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 6: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 6: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 6: 0/77	

447 UFQFPN5x5 32L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	500V	1	3	3	Lot 7: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 7: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 7: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 7: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 7: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 7: 0/77	

447 WLCSP49L, ASE KH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	500V	1	3	3	Lot 8: 0/3	
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 8: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 8: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 8: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 8: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 8: 0/77	

447 WLCSP49L, SCS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	500V	1	3	3	Lot 9: 0/3	
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 9: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 9: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 9: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 9: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 9: 0/77	

447 UFBGA5x5 64L, ATP AMKOR

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	500V	1	3	3	Lot 10: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 10: 0/308	
TC	JESD22-A104	Ta=-55/125°C Duration= 1000cyc ☒ After PC	1	77	77	Lot 10: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 10: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 10: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 10: 0/77	

447 TFBGA5x5 64L, ST MUAR

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ STM5.3.1	500V	1	3	3	Lot 11: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 11: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 11: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 11: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 11: 22W08	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 11: 22W08	

Table 7 - PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including -Wire bond shear -Wire bond pull	JESD22-B116 Mil Std 883-M2011	7	50	350	Lot 1: 0/50 Lot 2: 0/50 Lot 3: 0/50 Lot 5: 0/50 Lot 6: 0/50 Lot 7: 0/50 Lot 8: 0/50 Lot10: 0/50 Lot11: 0/50	

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid-state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Temperature Humidity Bake
JESD22-B116:	Wire Bond Shear Test method
Mil Std 883 M2011:	Bond Pull Strength

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HAST	Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Céline Navarro	Initial release	Division Quality Manager	RSST	Pascal NARCHE	14th September 2020
2.0	Cédric CHASTANG	Error Metal levels/Materials/Thicknesses information. (page 6) Changed: ALU --> COPPER ROUSSET + PCN13039 reference added in the title	Division Quality Manager	RSST	Pascal NARCHE	29th September 2021
3.0	Céline NAVARRO	Results updated for Back-end proliferation UFBGA 5x5 AMKOR (PCN12921) and target date for TFBGA 5x5 MUAR (PCN12922)	Division Quality Manager	RSST	Pascal NARCHE	24th January 2022

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PRODUCT/PROCESS CHANGE NOTIFICATION
PCN12922– Additional information

ST MUAR (Malaysia) TFBGA5x5 package assembly line – with additional ROUSSET source for STM32L05x and STM32L073x listed products

MDG - Microcontrollers Division (MCD)

What are the changes?

Changes described in table below:

	ST MUAR Back-End Site TFBGA5x5 Assembly Lines			
	Current lines			Added line
Product line	Crolles	Rousset		Rousset
Diffusion process variant	BEOL Copper	BEOL Aluminium		BEOL Copper

BEOL Copper = Back-End Of Line with 4 Metal copper + 1 Alu PAD

BEOL Aluminium = Back-End Of Line with 4 Metal Alu + 1 Alu PAD

How can the change be seen?

The standard marking is:

R code indicates die revision

Please refer to DataSheet for marking details.

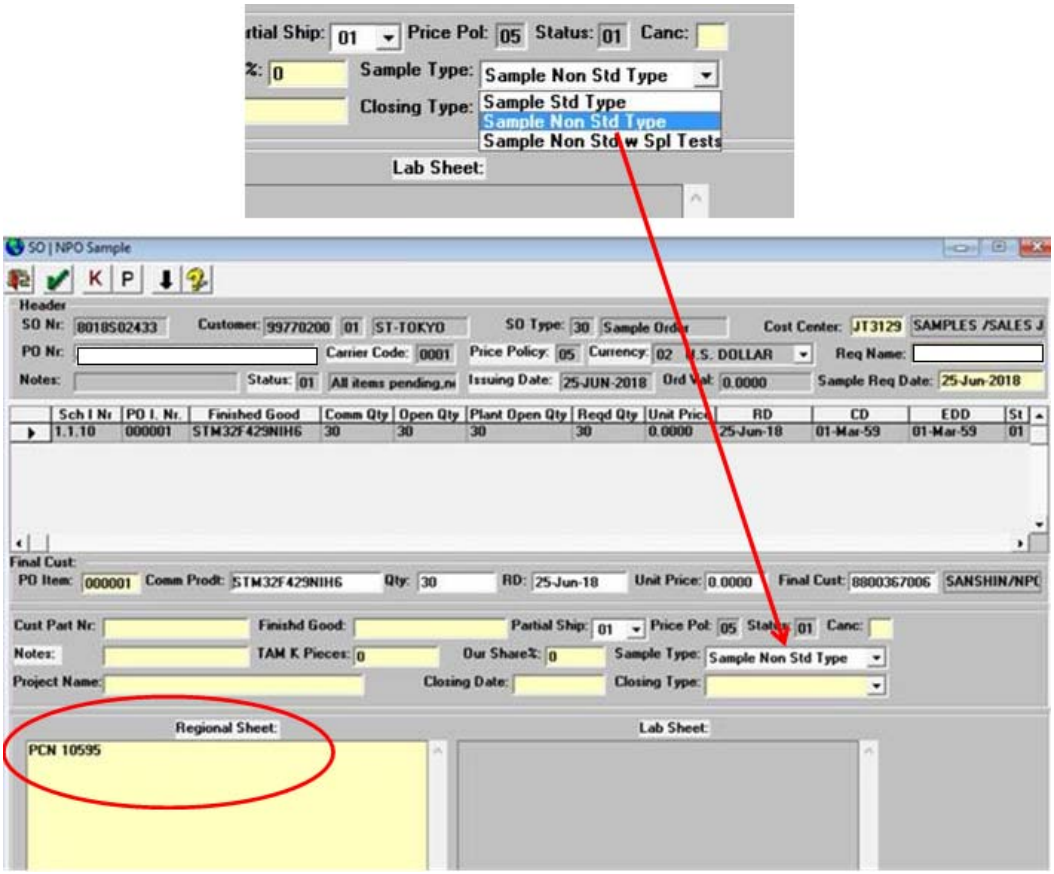
The marking is changing as follows:

Existing		Additional	
R code	Fab	R code	Fab
1	Crolles BEOL Copper	P	Rousset BEOL Copper
Z	Rousset BEOL Aluminium		

How to order samples?

For any sample request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "**PCN12922**" into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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