



## Public Products List

**PCI Title** : SEA05TR : Metal mask change

**PCI Reference** : IPD/16/9613

**PCI Created on** : 15-Jan-2016

**Subject** : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

SEA05TR		
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# Reliability Report

General Information	
Product Line	<i>U1M7</i>
Product Description	<i>ADVANCED CV/CC CONTROLLER</i>
Product division	<i>I&amp;PC</i>
Package	<i>SOT23 6L</i>
Silicon process technology	<i>BCD6S</i>

Locations	
Wafer fab location	<i>CATANIA</i>
Assembly plant location	<i>CARSEM M Malaysia</i>
Reliability assessment	<i>Pass</i>

## DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	26-Nov-15	12	<i>A. Spiezia</i>	Original document

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## 1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

## **2 RELIABILITY EVALUATION OVERVIEW**

### **2.1 Objectives**

This report contains the reliability evaluation performed on the U1M7 device diffused in CATANIA and assembled in SOT23 6L in CARSEM M Malaysia.

Considering that U1M7 device is an option of the already qualified **UQ23 device** (see report RR001609CS2047) and this option is marginal from reliability point of view, all positive results obtained from UQ23 can be extended by similarity to U1M7.

According to Reliability Qualification Plan, below is the list of the trials performed on reference device:

#### *Die Oriented Tests (performed on UQ23)*

- High Temperature Operating Life
- High Temperature Reverse Bias

#### *Package Oriented Tests (performed on equivalent Test Vehicle)*

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage

#### *Electrical Characterization (performed on UQ23)*

- ESD resistance test
- LATCH-UP resistance test

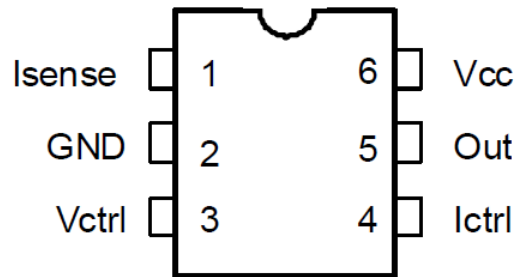
### **2.2 Conclusion**

Taking in account the results of the trials performed the U1M7 diffused in CATANIA and assembled in SOT23 6L in CARSEM M Malaysia can be qualified from reliability viewpoint.

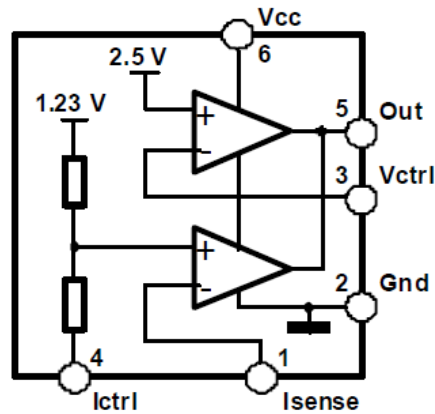
### 3 DEVICE CHARACTERISTICS

#### 3.1 Device description

##### 3.1.1 Pin connection



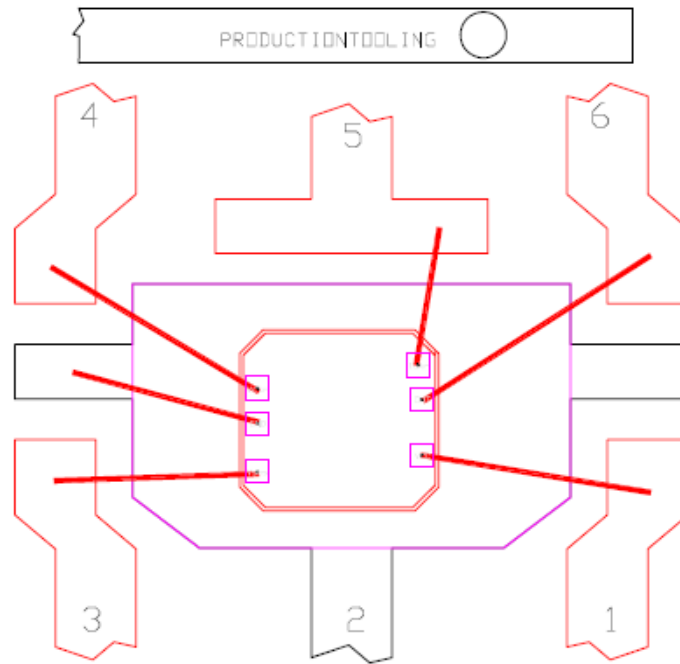
##### 3.1.2 Block diagram



### 3.1.3 Bonding diagram

FRAME PAD :  $\frac{39 \times 64 \text{ mils}}{0,981 \times 1,626 \text{ mm}}$

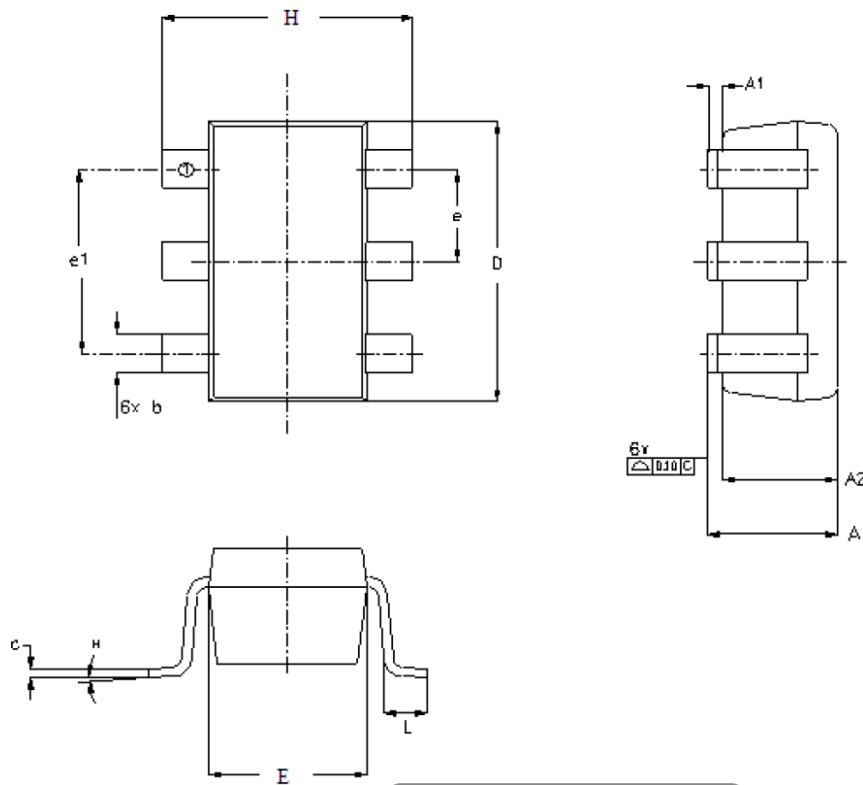
MAX DIE SIZE :  $\frac{29 \times 54 \text{ mils}}{0,727 \times 1,372 \text{ mm}}$





### 3.1.4 Package outline/Mechanical data

Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		0.9	1.45		0.035	0.057
A1		0	0.1		0	0.0039
A2		0.9	1.3		0.035	0.0512
b		0.35	0.5		0.014	0.02
c		0.09	0.2		0.004	0.008
D		2.8	3.05		0.11	0.120
E		1.5	1.75		0.059	0.0689
e	0.95			0.037		
H		2.6	3		0.102	0.118
L		0.1	0.6		0.004	0.024
$\theta$ (degrees)		0°	10°		0°	10°



## Traceability

<b>Wafer fab information</b>	
<b>Wafer fab manufacturing location</b>	<i>CATANIA</i>
<b>Wafer diameter</b>	<i>8 inches</i>
<b>Wafer thickness</b>	<i>280<math>\mu</math>m</i>
<b>Silicon process technology</b>	<i>BCD6S</i>
<b>Die finishing back side</b>	<i>Cr/Ni/Au</i>
<b>Die size</b>	<i>874 X 805<math>\mu</math>m</i>
<b>Bond pad metallization layers</b>	<i>Ti/AlCu/TiNARC</i>
<b>Passivation</b>	<i>TEOS/SiN/Polyimide</i>
<b>Metal levels</b>	<i>3</i>

<b>Assembly Information</b>	
<b>Assembly plant location</b>	<i>CARSEM M Malaysia</i>
<b>Package description</b>	<i>SOT23 6L</i>
<b>Die pad size</b>	<i>0.981 X 1.626mm</i>
<b>Molding compound</b>	<i>CEL8240 HF10LXC</i>
<b>Wires bonding materials/diameters</b>	<i>Au / 1mils</i>
<b>Die attach material</b>	<i>QMI519</i>
<b>Lead solder material</b>	<i>Sn</i>

## 4 TESTS RESULTS SUMMARY

### 4.1 Test plan and results summary

#### Die Oriented Tests

Test	Test short description (performed on UQ23)					
	Method	Conditions	Sample/ Lots	Lot Nb	Duration	Results Fail/SS
HTRB	High Temperature Reverse Bias					
		Tj=150°C Vin=36V, Vcc=6V, Vboot=42V	77	1	1000h	0/77
HTOL	High Temperature Operating Life					
	On chip-board	Tj=150°C Vcc=5V, Vin=21V	77	1	1000h	0/77

#### Package Oriented Tests

Test	Test short description (performed on equivalent Test Vehicle)					
	Method	Conditions	Sample/ Lots	Lot Nb	Duration	Results Fail/SS
PC	Pre-Conditioning: Moisture sensitivity level 1					
		168h 85°C/85% - 3 reflow PBT 260°C	100	1		0/100
AC	Autoclave					
	PC before	121°C 2atm	50	1	168h	0/50
TC	Temperature Cycling					
	PC before	Temp. range: -50/+150°C	50	1	1000cy	0/50
HTSL	High Temperature Storage Life					
	No bias	Tamb=150°C	50	1	1000h	0/50

#### Electrical Characterization Tests (performed on UQ23)

Test	Method	Conditions	Sample/ Lots	Number of lots	Duration	Results Fail/SS
ESD	Electro Static Discharge					
	Human Body Model	+/- 5000V	3	1		0/3
	Machine Mode	+/- 200V	3	1		0/3
	Charge Device Model	+/- 1500V	3	1		0/3
LU	Latch-Up					
	Over-voltage and Current Injection	Tamb=85°C Jedec78 – Level B	3	1		0/3

## **5 TESTS DESCRIPTION & DETAILED RESULTS**

### **5.1 Die oriented tests**

#### **5.1.1 High Temperature Operating Life**

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

#### **5.1.2 High Temperature Reverse Bias**

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

## **5.2 Package oriented tests**

### **5.2.1 Pre-Conditioning**

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.

The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

### **5.2.2 High Temperature Storage Life**

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.

The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

### **5.2.3 Thermal Cycles**

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.

Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

### **5.2.4 Autoclave**

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.

Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

## 5.3 Electrical Characterization Tests

### 5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up. The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
<i>IN low: 0V</i>	-100mA	Inom+100mA	V <sub>cc</sub> =54V
<i>IN high: 3.3V</i>	-100mA	Inom+100mA	V <sub>cc</sub> =54V

### 5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges. The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model**                      JEDEC STANDARD JESD22-A114  
CDF-AEC-Q100-002
- **Machine Model**                         JEDEC STANDARD EIA/JESD-A115  
CDF-AEC-Q100-003
- **Charge Device Model**                 ANSI/ESD STM 5.3.1 ESDA  
CDF-AEC-Q100-011