ADDING *GLOBAL FOUNDRIES* WAFER FOUNDRY FOR MANUFACTURING BCD6/20-40V AND BCD6S/20V-40V TECHNOLOGY II GROUP

WHAT is the change?

ST is pursuing the plan to rationalize the manufacturing processes to increase flexibility and capacity. Because of this, ST is announcing that the wafer foundry Global Foundries located in Singapore, will be used to manufacture BCD6 and BCD6S technology based products actually manufactured in M5 Wafer fab, Catania, Italy.
This notification is based and it is following the first announcement done on August 2014, same subject: IPG-IPC PCN 14/8673.
Wafer Fab Global Foundries has been already qualified by ST. This change will not affect EWS (Electrical Wafer Sort) activities and sites.

Technology Family	Commercial Products	Line codes	Packages	ASSY SITES
BCD6S-20V	ST1CC4	UI94	VFDFPN & SO8	CARSEM/ ST SHENZHEN
BCD6S-40V	LNBH29	UI86/UX55	QFN	CARSEM
	LNBH30	UI05	QFN	CARSEM

WHY:

In order to increase Advanced BCD technology manufacturing flexibility and capacity.

WHEN will this change occur?

The added use of the Global Foundries capacity will start from Q1-2016 for the above mentioned products. Because of the nature of the transfer, the different products will be implemented time by time and all within Q2-2016

HOW will the change be qualified?

- This change will be qualified using the standard STMicroelectronics procedures for quality and reliability.
  The validation of the transfer of these products is based on the already qualified products in Global Foundries, as mentioned on the previous PCN.
  This includes specific activities, including a full set of evaluations on selected test vehicles (TVs) which will cover: Wafer Parametric comparison (T84), EWS comparison, Electrical characterization at Final test, ESD/LU tests.
  Other products manufactured with same technology will be qualified by similarity (generic data).
  This transfer to Global Foundries will not modify the electrical, dimensional and thermal parameters for the product affected, keeping unchanged current description on relevant data sheets.

- Available qualification results, Samples availability and detailed Implementation schedule are reported in the below table. Concerning ST1CC4 in SO8 package the qualification result is attached to the present PCN.

Test Vehicles by Line codes	Product Family Code	Product family Description	PCN date	Qualification report/Samples availability	Forecasted First shipments
UI94	92	Power Conversion	Wk52	Attached for SO8 Wk15 for VFDFPN	Wk13-2016 Wk22-2016
UI86	I3	Hand Held & PMIC	Wk52	Wk05 for QFN 3*3 Wk15 for QFN4*4	Wk20-2016 Wk22-2016
UX55	I3	Hand Held & PMIC	Wk52	Wk05 for QFN 3*3 Wk15 for QFN 4*4	Wk20-2016 Wk22-2016
UI05	I3	Hand Held & PMIC	Wk52	Wk15 for QFN 4*4	Wk22-2016

ST Microelectronics – Agrate Site
Via C. Olivetti, 2 - 20041 Agrate Brianza (Milan) - Italy

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Report 341_2015_UI94ABF

Distribution List:	
Domenico GIUFFRIDA	Irene FERRERO
Carlo CODEGONI	Giulio GENGA
Alessandro PLATINI	Enzo SCARDAMAGLIA
Enzo NICOTRA	
Copy to:	
Luisa Fracassini	

ESD and Latch-up Test Report

Device: UI94ABF

RAWLINE CODE:	UI94AB
PACKAGE:	SO8
PROCESS:	BCD6S3m
DIFF. PLANT:	GF
INTERNAL CUSTOMER:	IPC

Author:	V. Sala
Approval:	A. Boroni

All equipment verifications and process flow are performed in agreement with internal Lab Procedure 7976412

Trials start date: 06-Nov-2015
Trials end date: 09-Nov-2015

Note:

ESD

REFERENCES

REFERENCE TABLE

ESD Model	International Standards	Internal spec. ST Microelectronics
HBM	ANSI/ESDA/JEDEC JS001	0060102 0061692
	AEC-Q100-002	
MM	EIA/JESD22-A115	
	AEC-Q100-003	
CDM	ANSI/ESD STM 5.3.1	
	ANSI/ESDA/JEDEC JS002	
	JESD22-C101	
	AEC-Q100-011	

FAILURE CRITERIA

-ANSI/ESDA/JEDEC

A part is defined as a failure if it fails the datasheet parameters using parametric and functional testing. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

-AEC

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

The ownership of final test and judgment is in charge of internal customer.

ENVIRONMENT AND EQUIPMENT

ENVIRONMENT

Temperature: 23° C +/- 5° C
Relative humidity: 50% +/- 10%

EQUIPMENT

Options set by default as indicated below except otherwise specified

MK2_ULP-19076
Shunt resistor (10kΩ): Yes
Discharge pins after zap: Yes (All)

ORION3-19037
Nitrogen: Yes
Monitored temperature and humidity: Yes
(T=23° C +/- 5° C; RH < 20%)
JS002 Correction Factor:0.76

Calibration evidences will be provided on demand.

CLASSIFICATION

CLASSIFICATION TABLE

ESD Model	Reference Standards	Equivalent Qualified Sample Size	Voltage	Table	Classification
HBM	ANSI/ESDA/JEDEC JS001-2014	3[B]	+/- 2000V	B	2
MM	EIA/JESD22-A115-C	3	+/- 200V[C]	-	NC
CDM	ANSI/ESD STM 5.3.1-2009	3	+/- 750V	-	C4

NOTE (If applicable, please see further for details):

A. Main differences from standard procedures.
B. Stress NOT performed in a cumulative way.
C. Lower Voltage skipped.
D. JS002: please refer to ENVIRONMENT AND EQUIPMENT section above for correction factor.
E. Pre and/or post stress only at RT.
F. Bake after stress.

TESTS CONDITIONS AND SEQUENCE

PIN GROUPS SUPPLY PINS

Group Name		Metal in Package, RDL/APL connection	Pin/Ball List
Supplies	GND	Y	2, 6, 7
	VINA		3
	VINSW		8

NOTE (If applicable):

A. For HBM/MM Test ONLY: grounded together (except for two pins tester) and tested only representative (first pin/ball in list).

PIN GROUPS NON-SUPPLY PINS/NON-CONNECT PINS

Group Name		Reference Power/GND Group	Metal in Package, RDL/APL connection	Paired IO list (Y/N)	Pin/Ball List
IO	EN				4
	FB				5
	SW				1

NOTE (If applicable):

A. For HBM/MM Test ONLY: grounded together (except for two pins tester) and tested only representative (first pin/ball in list).

HBM RESULTS TABLE

Sample n.	Precharge Voltage	Test method Configuration	ATE Failed Sample(s)	ATE Results (fail/good)
24, 25, 26	+/-2000V	All Pins VS GND	-	GOOD
27, 28, 29	+/-2000V	All Pins VS VINA	-	GOOD
30, 31, 32	+/-2000V	All Pins VS VINSW	-	GOOD
33, 34, 35	+/-2000V	IO VS IO	-	GOOD
36, 37, 38	+/-1000V	Cumulative Stress	-	GOOD

MM RESULTS TABLE

Sample n.	Precharge Voltage	Test method Configuration	ATE Failed Sample(s)	ATE Results (fail/good)
39, 40, 41	+/-200V	Cumulative Stress	-	GOOD
42, 43, 44	+/-100V	Cumulative Stress	-	GOOD

CDM RESULTS TABLE

Sample n.	Precharge Voltage	Test method Configuration	ATE Failed Sample(s)	ATE Results (fail/good)
12, 13, 14	+/-250V	All Pins	-	GOOD
15, 16, 17	+/-500V	All Pins	-	GOOD
18, 19, 20	+/-750V	All Pins	-	GOOD
21, 22, 23	+/-750V	Corner pins	-	GOOD

NOTE (in case of test done using different standard):

A. **ANSI/ESD STM 5.3.1-2009**
B. **JESD22-C101-F**
C. **AEC-Q100-011-C**
D. **ANSI/ESDA/JEDEC JS001-2014**

LATCH-UP

REFERENCES

REFERENCE TABLE

Model	International Standards	Internal spec. ST Microelectronics
LU	JESD78x	0018695 0061692
	AEC-Q100-004	

FAILURE CRITERIA

A device that fails one or more of the following conditions is considered a failure:

- Device does not pass the test requirements defined in international specification
- Device no longer meets functional, parametric or I/V requirements of the device specification (room and/or hot test as per reference standard specification).

The ownership of final test and judgment is in charge of internal customer.

ENVIRONMENT AND EQUIPMENT

ENVIRONMENT

Temperature: 23° C +/- 5° C
Relative humidity: 50% +/- 10%

EQUIPMENT

Options set by default as indicated below except otherwise specified

MK2-17991

Calibration evidences will be provided on demand.

CLASSIFICATION

CLASSIFICATION TABLE

Test	Reference Standards	Equivalent Qualified Sample Size	Immunity Level	Temperature	Clamp
Negative I- Test	EIA/JESD78D	3[B]	100mA	Class II(85°C)	Voltage Clamp @ minimum between AMR, MSV, Jedec 78D std clamp
Positive I- Test	EIA/JESD78D	3[B]	100mA	Class II(85°C)	
Overvoltage	EIA/JESD78D	3[B]	1.5 x VDD or MSV or AMR, whichever is less	Class II(85°C)	100 mA + Inom or 1.5x Inom whichever is greather

NOTE (If applicable, please see further for details):

A. Device doesn't meet AEC-Q100 requirements.
B. Stress NOT performed in a cumulative way.
C. Test performed also at RT.

TESTS CONDITIONS AND SEQUENCE

PIN GROUPS SUPPLY PINS

Group Name	Type	Pin/Ball List
GND	GROUND	7, 6, 2
V18v	POWER	3, 8

PIN GROUPS NON-SUPPLY PINS/NON-CONNECT PINS

Group Name	Type	Pin/Ball List
HIGH 3.3v	INPUT	5
HIGH 18v	INPUT	4
out 18v	OUTPUT	1

VECTOR

Pin/Ball	High/Low Level	Threshold	Frequency
-	-	-	-

(See annex spreadsheet for vector details)

LATCH-UP RESULTS TABLE T_{DUT} = 85°C

Sample N.	Trigger Condition	Input	ESD lab Results	ATE Failed Sample(s)	ATE Results (Fail/Good)
50, 47, 46	-100mA	-	NO latch	-	GOOD
49, 47, 46	+100mA	-	NO latch	-	GOOD
48, 47, 46	Overvoltage	-	NO latch	-	GOOD

(See further for test summary and annex spreadsheet for measurement details)

LATCH UP SUMMARY TABLE

Device	Test	Pin	Summary
46	inj+_85C	5	Sourced or Sinked Current less than 20% than desired @ Clamp
47	inj+_85C	5	Sourced or Sinked Current less than 20% than desired @ Clamp
49	inj+_85C	5	Sourced or Sinked Current less than 20% than desired @ Clamp
46	ove _85C	V18v	Current less than 20% than desired in Overvoltage Test
47	ove _85C	V18v	Current less than 20% than desired in Overvoltage Test
48	ove _85C	V18v	Current less than 20% than desired in Overvoltage Test

(The aim of summary is to highlight most common issues. Please check excel spreadsheet for complete test results.)

Public Products List

PCN Title : ADDING "GLOBAL FOUNDRIES" WAFER FOUNDRY FOR MANUFACTURING BCD6/20-40V AND BCD6S/20V-40V TECHNOLOGY
II GROUP

PCN Reference : IPD/16/9598

PCN Created on : 22-Dec-2015

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

LNBH29PTR	ST1CC40PUR	LNBH29EQTR
ST1CC40DR	LNBH29QTR	LNBH29EPTR
LNBH30QTR		

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