

Reliability Report

QUALIFICATION PROCESS CHANGE FE

New DIE IN HBIP40, Capacity Change from Oxide to junction

TV: LX0501 – L7805CV – TO220 SINGLE GAUGE

General Information

| | |
|----------------------------|--|
| Product Line | LX0501 |
| Product Description | Positive Voltage Regulator |
| P/N | lcs L7805CV |
| Product Group | IPD IPC |
| Product division | IND.& POWER CONV. Voltage Vregulator & Vref |
| Package | TO220 SG |
| Silicon Process technology | HBIP40 |

Locations

| | |
|------------------------|-----------------------------|
| Wafer fab | Ang Mo Kio (Singapore) |
| Assembly plant | ST Shenzhen |
| Reliability Lab | IPD Catania Reliability Lab |
| Reliability assessment | Pass |

DOCUMENT INFORMATION

| Version | Date | Pages | Prepared by | Approved by | Comment |
|---------|----------|-------|---------------------------------------|-----------------|--------------|
| 1.0 | MAY-2015 | 7 | Vito Gisabella Giuseppe Giacobello | Giovanni Presti | Final report |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|--------------------|---|
| JESD47 | Stress-Test-Driven Qualification of Integrated Circuits |

2 GLOSSARY

| | |
|-----|-------------------|
| DUT | Device Under Test |
| SS | Sample Size |

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Following Divisional Commitments towards a continuous improvement philosophy, we have replaced the old Oxide Capacitor structure with the new integrated Junction Capacitor, as a consequence of an improved product quality.

TV: L7805CV, TO220 SG, HBIP40 (new integrated Junction Capacitor).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The L78xx series of three-terminal positive regulators is available in several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shutdown and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable

4.1 Construction note

| L7805CV-LX0501 | |
|---|----------------------|
| Wafer/Die fab. information | |
| Wafer fab manufacturing location | Singapore Ang Mo Kio |
| Technology | HBIP40V |
| Die finishing back side | Cr/NiV/Au |
| Die size | 1320, 1630 micron |
| Passivation type | P-Vapox/Nitride |
| Wafer Testing (EWS) information | |
| Electrical testing manufacturing location | Ang Mo Kio EWS |
| Tester | ETS 300 |
| Assembly information | |
| Assembly site | Shenzhen B/E |
| Package description | TO220 SG |
| Molding compound | Epoxy |
| Frame material | Bare copper |
| Die attach material | PREFORM |
| Wires bonding materials/diameters | WIRE Cu D2 |
| Final testing information | |
| Testing location | Shenzhen B/E |

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

| Lot # | Package | Product Line | Comments |
|-------|----------|--------------|----------|
| 1 | TO220 SG | LX0501 | |

5.2 Test plan and results summary

| Test | | Std ref. | Conditions | SS | Steps | Failure/SS | Note |
|------------------------|--|--------------------------|------------------------------------|----|--------|------------|---------------------------|
| | | | | | | 1°LOTTO | |
| Die Oriented Tests | | | | | | | |
| HTOL | | JESD22 A-108 | Tj = 125°C Vcc= +35V | | 168 H | 0/77 | |
| | | | | | 500 H | 0/77 | |
| | | | | | 1000 H | 0/77 | |
| HTSL | | JESD22 A-103 | Ta = 150°C | | 168 H | 0/45 | Engineering Evaluation |
| | | | | | 500 H | 0/45 | |
| | | | | | 1000 H | 0/45 | |
| Package Oriented Tests | | | | | | | |
| AC | | JESD22 A-102 | Pa=2Atm / Ta=121°C | | 96 H | 0/77 | Engineering Evaluation |
| | | | | | 168 H | 0/77 | |
| TC | | JESD22 A-104 | Ta = -65°C to 150°C | | 100 CY | 0/77 | |
| | | | | | 200 CY | 0/77 | |
| | | | | | 500 CY | 0/77 | |
| THB | | JESD22 A-101 | Ta = 85°C, RH = 85%, Vcc1= +24V | | 168 H | 0/77 | |
| | | | | | 500 H | 0/77 | |
| | | | | | 1000 H | 0/77 | |
| Other Tests | | | | | | | |
| ESD | | ANSI/ESDA/JEDEC JS001 | HBM +/- 2000V | 3 | Pass | | |
| | | ANSI/ESD S5.3.1 | CDM 500V | 3 | Pass | | |

6 ANNEXES

6.1 Tests Description

| Test name | Description | Purpose |
|--|--|---|
| Die Oriented | | |
| HTOL High Temperature Bias | The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition. | To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults. |
| HTSL High Temperature Storage Life | The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature. | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding. |
| Package Oriented | | |
| AC Auto Clave (Pressure Pot) | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |
| TC Temperature Cycling | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation. |
| THB Temperature Humidity Bias | The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity. | To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence. |
| Other Test | | |
| ESD Electro Static Discharge | The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model HBM: Human Body Model | To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge. |