Reliability Qualification Report
SO16N Leadframe Strip Change in Amkor (From HD to XD) - AMKOR PCN 140501

General Information	
Product Line	MU6203
Product From	9RQ7*MU62BBX
Process Plan	A2 - BCD6 / A5 – BCD OFFLINE
Package Technology	Q7 SO 16 .15 TO JEDEC MS-012

Locations	
Wafer Fab Location	CM5F - Catania CTM8
Assembly Plant Location	ZY1A SC AMKOR ATP1 - PHILIPPINES
Testing Plant	SH1T ST SHENZHEN -CHINA 3068
Reliability Assessment	ST MUAR (QA RELIABILITY LAB)

Issued By: Mohd Ibrahim GHAZALI

Approved By: Francesco VENTURA

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document Reference	Short Description
AEC-Q100	Stress test qualification for integrated circuits
SOP 2.6.11	Project management for product development
SOP 2.6.19	Front-end technology platform development & qualification
SOP 2.6.2	Internals change management
SOP 2.6.7	Product maturity level
SOP 2.6.9	Package and process maturity management in Back End
SOP 2.7.5	Automotive products definition and status
0061692	Reliability tests and criteria for product qualification
8160601	Internal reliability evaluation report template
8161393	General specification for product development

2 TEST GLOSSARY

TEST NAME	DESCRIPTION
PC (JL3)	Preconditioning (Solder Simulation)
TC	Temperature Cycling
AC or PPT	Autoclave or Pressure Pot Test
HTSL	High Temperature Storage Life

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The aim of this report is to present the results of the reliability assessment evaluation performed on L6591TR-9LF/ or L6591-9LF/ (9RQ7*MU62BBX) – the Lead frame strip changed in Assembly Plant AMKOR ATP1 – PHILIPPINES (from HD to XD), impact on package Q7 SO 16 .15 TO JEDEC MS-012 (with reference to AMKOR PCN 140501).

The main purpose is to qualify XD Leadframe as a new strip for Q7 SO 16 .15 TO JEDEC MS-012.

L6591TR-9LF/ or L6591-9LF/ is processed in A2 - BCD6 & A5 - BCD OFFLINE, diffused in CM5F - Catania CTM8 and assembled in AMKOR ATP1 – PHILIPPINES.

For the reliability assessment evaluation the following test were carried out:

- Preconditioning JL3 (3X Reflow)
- Temperature Cycling (TC)
- Autoclave / Pressure Pot Test (AC / PPT)
- High Temperature Storage Life (HTSL)

3.2 Conclusions

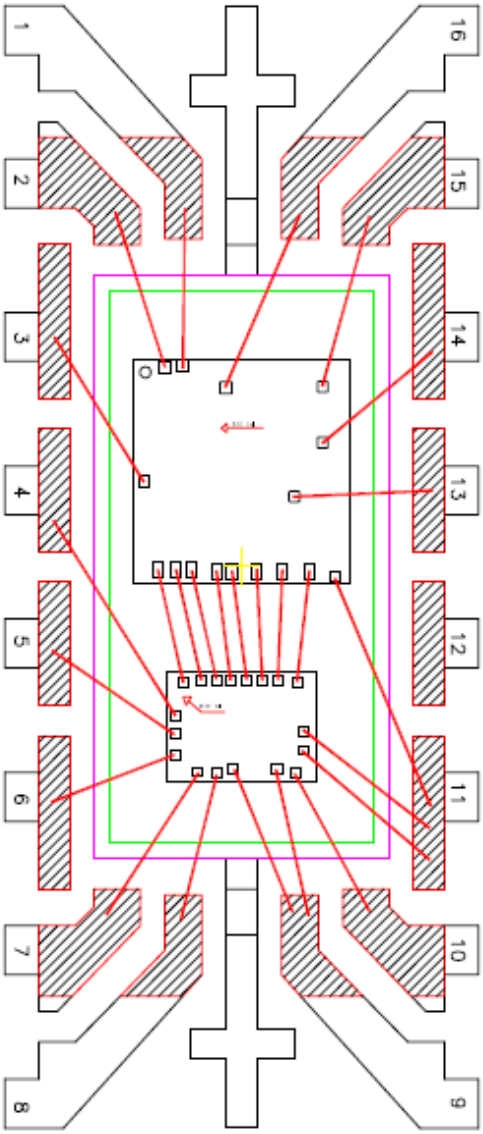
All reliability tests have been completed with positive results (no any electrical failure that can be link to new Lead-frame strip changed from HD to XD). Package oriented test and destructive physical analysis - SAM also have not put in evidence any criticality to package robustness.

4 DEVICE CHARACTERISTICS

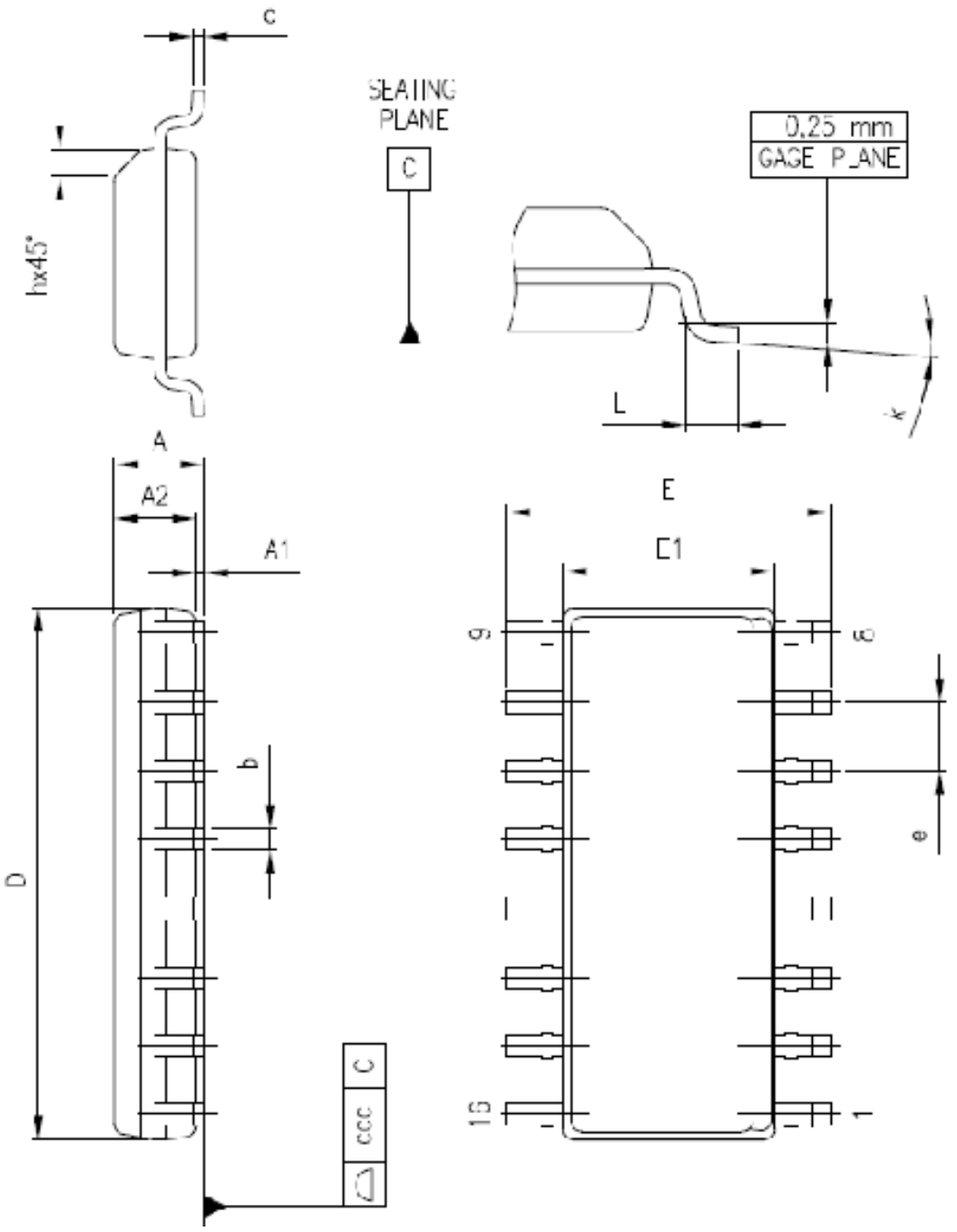
4.1 Bond Diagram

FRAME PAD : 96 x 190 mils / 2,438 x 4,826 mm

MAX DIE SIZE : 86 x 180 mils / 2,184 x 4,572 mm



Package Outline / Mechanical Data



4.2 Package Outline / Mechanical Data

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.75	1.43	1.55	1.68	
A1	0.10		0.25	0.12	0.15	0.18	
A2	1.25			1.48	1.52	1.56	
b	0.31		0.51	0.375	0.40	0.425	
c	0.17		0.25			0.238	
D	9.80	9.90	10.00	9.82	9.85	9.88	(1) (3)
E	5.80	6.00	6.20	5.90	6.00	6.10	
E1	3.80	3.90	4.00	3.87	3.90	3.93	(2) (3)
e		1.27			1.27		
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	0.585	0.635	0.685	
k	0		8	2	4	8	DEGREES
ccc			0.10			0.04	

4.3 Traceability

Wafer Fab Information	
Wafer fab manufacturing location	CM5F - Catania CTM8
Wafer diameter	6 inch
Wafer thickness (XUL25CB5)	375+/-20 UM
Silicon process technology	A2 - BCD6
Die finishing back side	RAW SILICON SINGLE GRIND (TYPICA
Die finishing front side	TEOS /SiN / Polyimide
Die size	81,81 UM
Wafer Thickness (XU335AB6)	375+/- UM
Silicon process technology	A5 - BCD OFFLINE
Die finishing back side	CHROMIUM / NICKEL
Die finishing front side	SiN (nitride)
Die size	90,90 UM

Assembly Information	
Assembly plant location	ZY1A SC AMKOR ATP1 - PHILIPPINES
Package description	Q7 SO 16 .15 TO JEDEC MS-012
Molding compound	Sumitomo G600
Wire bonding materials/diameters	Au 1.0 Mils
Die attach material	Ablestik 8290
Lead frame material	XDLF SO S 16L96*190 C194 DR AG XDIDF #101385539

Final Testing Information	
Electrical testing location	SH1T ST SHENZHEN -CHINA
Tester	ASL1K

5. TEST RESULTS SUMMARY

5.1 Lot Information

Lot #	Diffusion Lot	Lot Details / Trace Code	Assy Lot Id	Testing Lot Id
1		GK6270WY01 / 7B623728	GK6270WY01	GK6270WY01

5.2 Test Plan and Results Summary (Electrical Test)

Reliability Test Status						
No	Test Name	Prec	Condition/ Method	Steps	Fails/SS	Notes
					Lot 1	
1	PC (JL3)		Bake 24hrs @ 125°C Soak 192hrs @ 30°C/60%RH Reflow Profile = J-STD-020D (Tmax = 260°C)	Final	0 / 164	Pass
2	TC	Yes	Test Conditions = -65°C / +150°C	200cyc	0 / 77	Pass
				500cyc	0 / 76	Pass
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 77	Pass
				168hrs	0 / 77	Pass
4	HTS	No	Test Conditions = Ta = +150°C	500hrs	0 / 77	Pass
				1000hrs	0 / 77	Pass

NOTES

All units electrically tested good (all Pass) after each reliability readout. No any electrical failure found that can be link to the weakness of the assembly process or due the Lead-Frame Strip change from HD to XD in Amkor Philippines (ATP1).

5.3 Test Plan and Results Summary (SAM Analysis)

Reliability Test Status						
No	Test Name	Prec	Condition/ Method	Steps	Fails/SS	Notes
					Lot 1	
1	PC (JL3)		Bake 24hrs @ 125°C Soak 192hrs @ 30°C/60%RH Reflow Profile = J-STD-020D (Tmax = 260°C)	Final	0 / 60	No Delam
2	TC	Yes	Test Conditions = -65°C / +150°C	200cyc	0 / 20	No Delam
				500cyc	0 / 19	No Delam
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 20	No Delam
				168hrs	0 / 20	No Delam
5	HTS	No	Test Conditions = Ta = +150°C	500hrs	0 / 20	No Delam
				1000hrs	0 / 20	No Delam

NOTES

SAM analysis did not reveal any delam on Die Attach Material (DAM) & Die / Molding Compound (Die Top) on sampling basis 20 pcs for each reliability test The Lead and die-paddle delam (die-pad front side / molding compound) after Reliability (TC Trial) is an intrinsic problem of this package and not related to the change being qualified.

All units with or without Lead delam passed the electrical testing after TC200 & TC500.

6. TESTS DESCRIPTION

6.1 Package tests description

TEST NAME	DESCRIPTION	PURPOSE
PC (JL3) Preconditioning MSL3 (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting after storage in a control moisture absorption.	As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are link to metal displacement, dielectric cracking, molding compound delamination, wire bonds failure, die crack.
AC or PPT Autoclave / Pressure Pot Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max temperature allowed by the package materials, sometimes higher than the max operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

Reliability Qualification Report
SO14N Leadframe Strip Change in Amkor (From HD to XD) - AMKOR PCN 140501

General Information	
Product Line	MV0301
Product From	BRK7*MV03AAX
Process Plan	
Package Technology	K7 SO 14 .15 TO JEDEC MS-012

Locations	
Wafer Fab Location	AM6F - Singapore 6"
Assembly Plant Location	ZY1A SC AMKOR ATP1 - PHILIPPINES
Testing Plant	MU1T ST MUAR - MALAYSIA
Reliability Assessment	ST MUAR (QA RELIABILITY LAB)

Issued By: Mohd Ibrahim GHAZALI

Approved By: Francesco VENTURA

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SOP 2.6.9	Package and process maturity management in Back End
SOP 2.7.5	Automotive products definition and status
0061692	Reliability tests and criteria for product qualification
8160601	Internal reliability evaluation report template
8161393	General specification for product development

2 TEST GLOSSARY

TEST NAME	DESCRIPTION
PC (JL3)	Preconditioning (Solder Simulation)
TC	Temperature Cycling
AC or PPT	Autoclave or Pressure Pot Test
HTSL	High Temperature Storage Life

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The aim of this report is to present the results of the reliability assessment evaluation performed on L6564HTR-2/ or L6564H-2/ (BRK7*MV03AAX) – the Lead-frame strip changed in Assembly Plant AMKOR ATP1 – PHILIPPINES (from HD to XD), impact on package K7 SO 14 .15 TO JEDEC MS-012 (with reference to AMKOR PCN 140501).

The main purpose is to qualify XD Lead-frame as a new strip for K7 SO 14 .15 TO JEDEC MS-012.

L6564HTR-2/ or L6564H-2/ is processed in A5 - BCD OFFLINE & A7 - BCD2S, diffused in AM6F - Singapore 6" and assembled in AMKOR ATP1 – PHILIPPINES.

For the reliability assessment evaluation the following package oriented test were carried out:

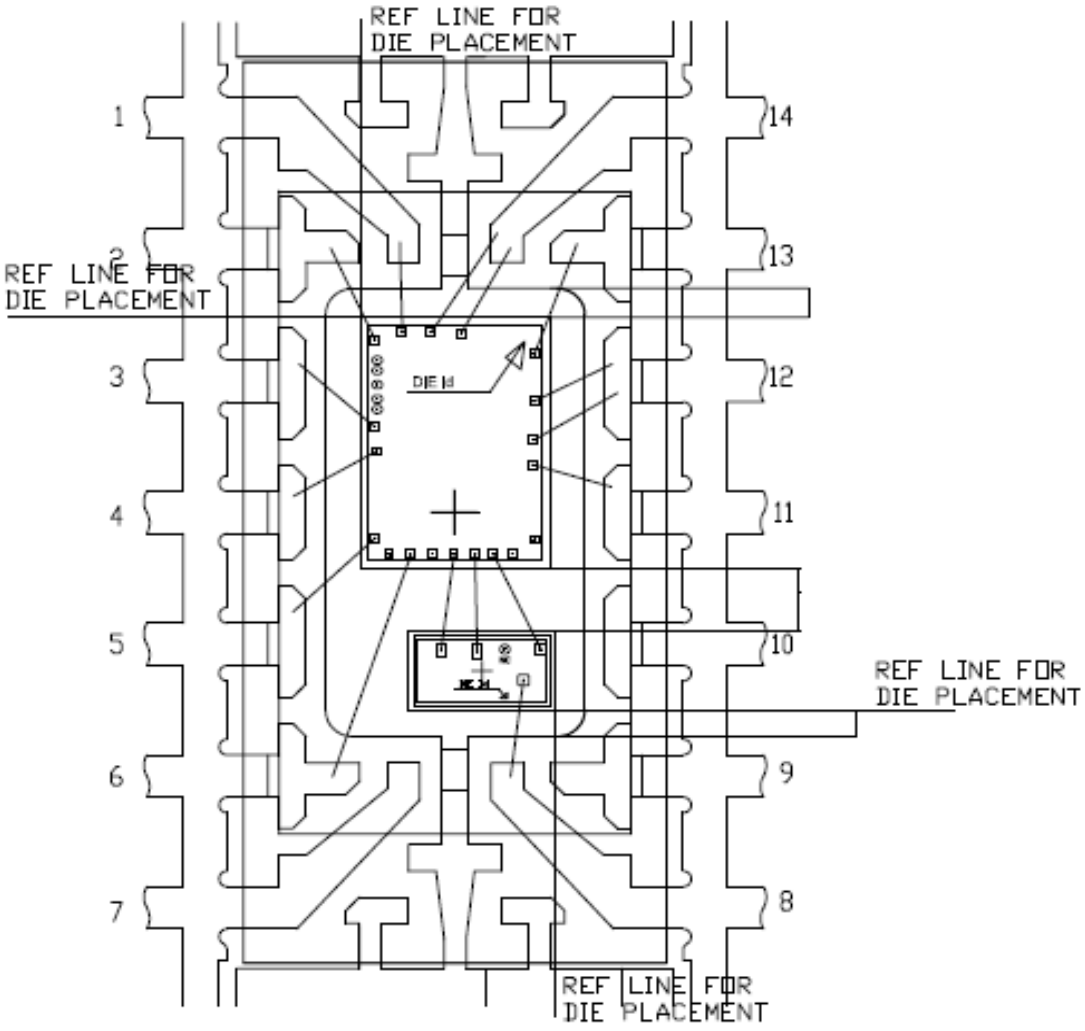
- Preconditioning JL3 (3X Reflow)
- Temperature Cycling (TC)
- Autoclave / Pressure Pot Test (AC / PPT)
- High Temperature Storage Life (HTSL).

3.2 Conclusions

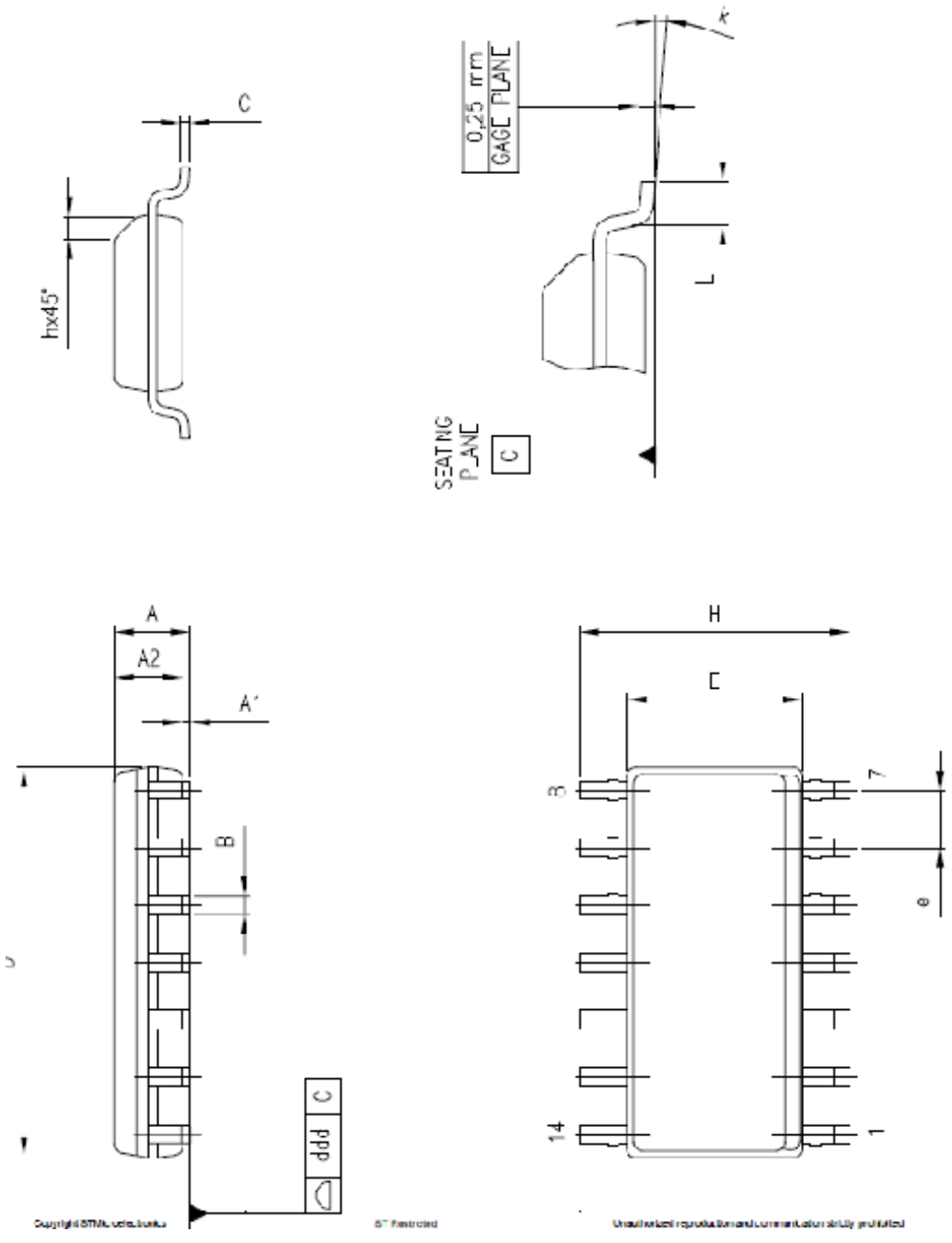
All reliability tests have been completed with positive results (no any electrical failure that can be link to new Lead-frame strip changed from HD to XD). Package oriented test and destructive physical analysis - SAM also have not put in evidence any criticality to package robustness.

4 DEVICE CHARACTERISTICS

4.1 Bond Diagram



4.2 Package Outline / Mechanical Data



4.2 Package Outline / Mechanical Data

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A	1.35		1.75			1.75	
A1	0.10		0.25	0.10	0.15	0.20	
A2	1.10		1.65	1.48	1.52	1.60	
B	0.33		0.51	0.35	0.40	0.455	
C	0.19		0.25	0.19	0.20	0.238	
D	8.55		8.75	8.60	8.65	8.70	(1)
E	3.80		4.00	3.80	3.90	4.00	
e		1.27			1.27		
H	5.80		6.20	5.90	6.00	6.10	
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	0.50	0.635	0.685	
k	0		8	2	4	8	DEGREES
ddd			0.10			0.04	

NOTES:

(1) – Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

(2) – Drawing dimensions include Single and Matrix versions.

4.3 Traceability

Wafer Fab Information	
Wafer fab manufacturing location	AM6F - Singapore 6"
Wafer diameter	6 inch
Wafer thickness (XU327AB6)	254+/-20 UM
Silicon process technology	A5 - BCD OFFLINE
Die finishing back side	CHROMIUM / NICKEL
Die finishing front side	SiN (Nitride)
Die size	
Wafer Thickness (XUE40AE6)	375+/-20 UM
Silicon process technology	A7 - BCD2S
Die finishing back side	CHROMIUM / NICKEL / GOLD
Die finishing front side	P-VAPOX(SiO2) / NITRIDE (SiN)
Die size	81,81 UM

Assembly Information	
Assembly plant location	ZY1A SC AMKOR ATP1 - PHILIPPINES
Package description	K7 SO 14 .15 TO JEDEC MS-012
Molding compound	SUMITOMO G600
Wire bonding materials/diameters	Au 1.0 Mils
Die attach material	ABLESTIK 8290
Lead frame material	LF SO S 14L 95*170 C194 TLPPF 150B XD

Final Testing Information	
Electrical testing location	SH1T ST SHENZHEN - CHINA 3068
Tester	ASL1K

5. TEST RESULTS SUMMARY

5.1 Lot Information

Lot #	Diffusion Lot	Lot Details / Trace Code	Assy Lot Id	Testing Lot Id
1		GK6201BS01 / 7B618482	GK6201BS01	GK6201BS01

5.2 Test Plan and Results Summary (Electrical Test)

Reliability Test Status						
No	Test Name	Prec	Condition/ Method	Steps	Fails/SS	Notes
					Lot 1	
1	PC (JL3)		Bake 24hrs @ 125°C Soak 192hrs @ 30°C/60%RH Reflow Profile = J-STD-020D (Tmax = 260°C)	Final	0 / 164	Pass
2	TC	Yes	Test Conditions = -65°C / +150°C	500cyc	0 / 77	Pass
				1000cyc	0 / 77	Pass
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 77	Pass
				168hrs	0 / 77	Pass
4	HTS	No	Test Conditions = Ta = +150°C	500hrs	0 / 77	Pass
				1000hrs	0 / 77	Pass

NOTES

All units electrically tested good (all Pass) after each reliability readout. No any electrical failure found that can be link to the weakness of the assembly process or due the Lead-Frame Strip change from HD to XD in Amkor Philippines (ATP1).

5.3 Test Plan and Results Summary (SAM Analysis)

Reliability Test Status						
No	Test Name	Prec	Condition/ Method	Steps	Fails/SS	Notes
					Lot 1	
1	PC (JL3)		Bake 24hrs @ 125°C Soak 192hrs @ 30°C/60%RH Reflow Profile = J-STD-020D (Tmax = 260°C)	Final	0 / 60	No Delam
2	TC	Yes	Test Conditions = -65°C / +150°C	500cyc	0 / 20	No Delam
				1000cyc	0 / 20	No Delam
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 20	No Delam
				168hrs	0 / 20	No Delam
				1000hrs	0 / 20	No Delam
5	HTS	No	Test Conditions = Ta = +150°C	500hrs	0 / 20	No Delam
				1000hrs	0 / 20	No Delam

NOTES

SAM analysis did not reveal any delam on Die Attach Material (DAM) & Die / Molding Compound (Die Top) on sampling basis 20 pcs for each reliability test The Lead and die-paddle delam (die-pad front side / molding compound) after Reliability (TC Trial) is an intrinsic problem of this package and not related to the change being qualified.

All units with or without Lead delam passed the electrical testing after TC500 & TC1000 and no lifted weld or broken weld during pull test after TC1000.

6. TESTS DESCRIPTION

6.1 Package tests description

TEST NAME	DESCRIPTION	PURPOSE
PC (JL3) Preconditioning MSL3 (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting after storage in a control moisture absorption.	As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are link to metal displacement, dielectric cracking, molding compound delamination, wire bonds failure, die crack.
AC or PPT Autoclave / Pressure Pot Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max temperature allowed by the package materials, sometimes higher than the max operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

Reliability Report

General Information	
Product Line	*MT57 (UAF0+U343)*
Product Description	*Ballast dimmable controller for OSRAM*
Product division	*I&PC*
Package	*SO16N*
Silicon process technology	*CATANIA (UAF0) + ANG MO KIO(U343)*

Locations	
Wafer fab location	*CATANIA (UAF0) + ANG MO KIO(U343)*
Assembly plant location	*AMKOR ATP1- PHILIPPINES*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	10-Oct-16	15	A. SPIEZIA	LeadFrame Strip change in Amkor

Approved by

G. CAPODICI

Table of Contents

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of the MT57 (UAF0+U343) device diffused in CATANIA (UAF0) + ANG MO KIO(U343) and assembled in SO16N in AMKOR ATP1-PHILIPPINES, in the overall plan of LeadFrame Strip change in Amkor (AMG/16/9945).

Below is the list of the overall trials performed on samples with new LeadFrame:

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life

2.2 Conclusion

Taking in account the results of the trials performed **the MT57 (UAF0+U343) diffused in CATANIA (UAF0) + ANG MO KIO(U343) assembled in SO16N in AMKOR ATP1-PHILIPPINES can be qualified from reliability viewpoint.**

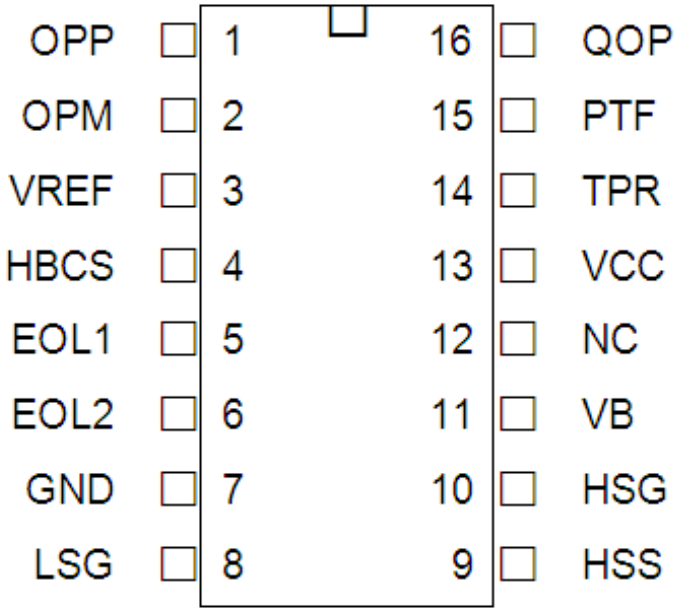
3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Generalities

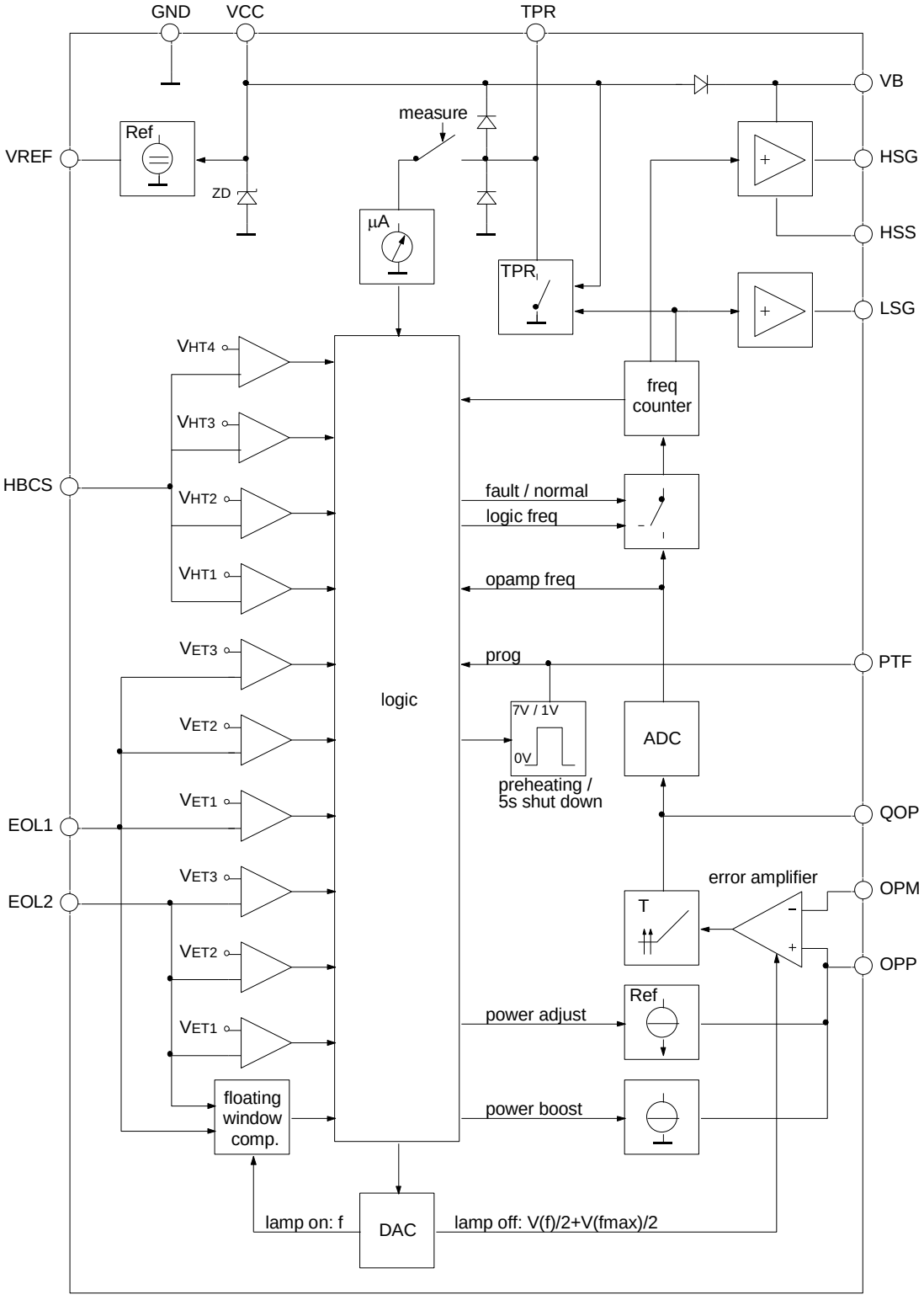
This IC is designed to drive the MOS half bridge of dimmable electronic ballast, a MOS transistor for preheating the filaments of a fluorescent lamp and a PNP transistor for the controlled Vcc supply of the IC. It is suitable for ballasts in “lamp to ground” topology as well as for ballasts in “capacitor to ground” topology.
All necessary monitoring functions like filament detection, ignition control, capacitive mode protection, end of life detection, hard rectifying protection and output voltage limitation are included as well as an error amplifier and a voltage reference.

3.1.2 Pin connection

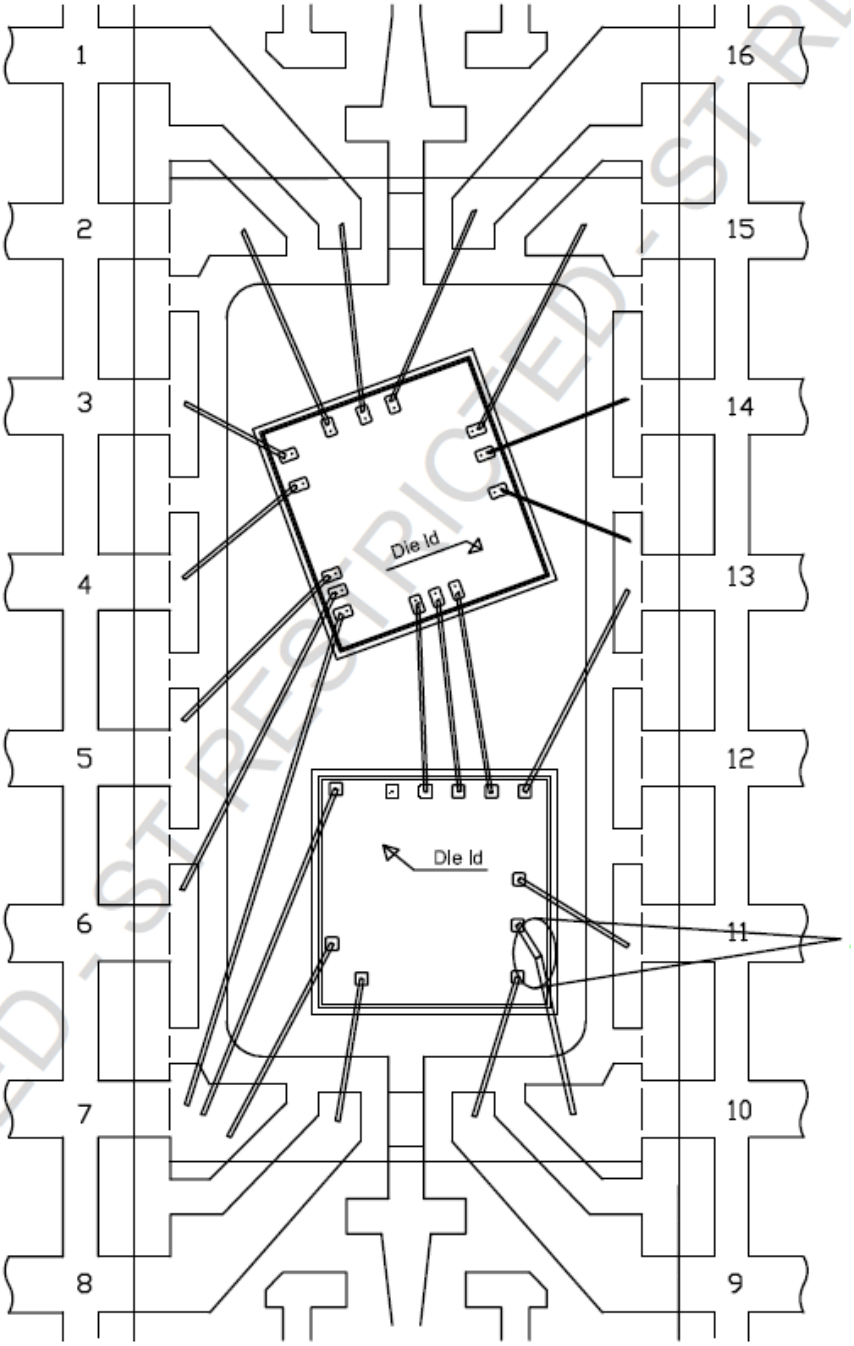


symbol	pin	description
OPP	1	Non inverting input of the error amplifier
OPM	2	Inverting input of the error amplifier
VREF	3	3.3V reference voltage
HBCS	4	Half bridge current sensing
EOL1	5	End of life, filament detection and control of the HBCS thresholds
EOL2	6	End of life, filament detection and control of the HBCS thresholds
GND	7	Ground
LSG	8	Low side gate driver output and clock output for programming and power adjustment
HSS	9	High side driver floating reference
HSG	10	High side gate driver output
VB	11	Bootstrapped supply voltage
NC	12	Not connected
VCC	13	Supply voltage
TPR	14	Two point regulator for Vcc supply
PTF	15	Digital input for programming and power adjustment, control of the preheat MOS
QOP	16	Error amplifier output and frequency control input

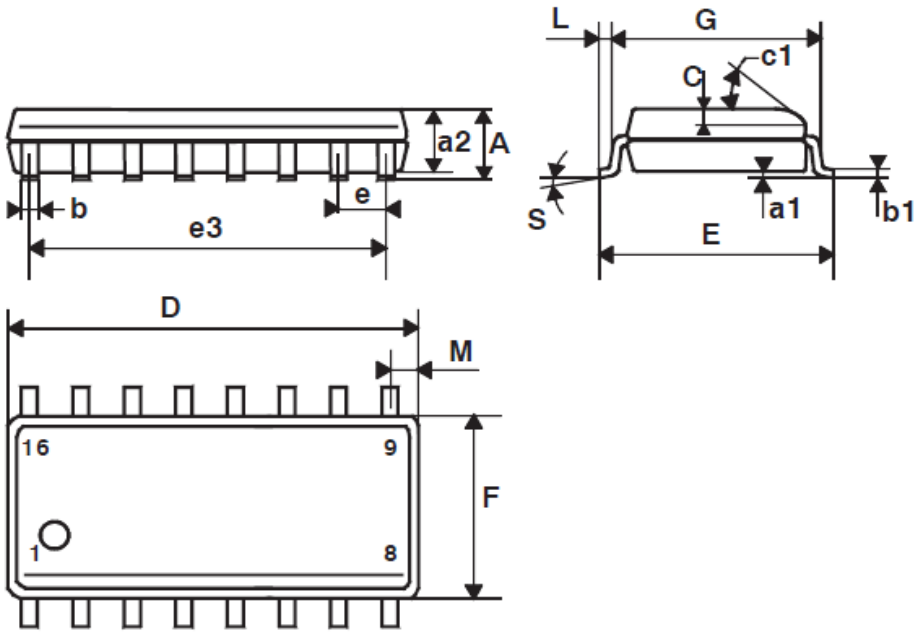
3.1.3 Block diagram



3.1.4 Bonding diagram: MT57ADA – rotated die version



3.1.5 Package outline/Mechanical data



REF.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45°(typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.158
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.62			0.024
S	8°(max.)					

3.2 Traceability

Wafer fab information for UAF0	
Wafer fab manufacturing location	*CATANIA M5*
Wafer diameter	*8 inches*
Wafer thickness	*375 µm*
Silicon process technology	*BCD8AS*
Die finishing back side	*CHROMIUM/NICKEL/GOLD*
Die size	*1701X1784 µm*
Bond pad metallization layers	*AlCu*
Passivation	*NITRIDE*
Metal levels	*4*
Wafer fab information for U343	
Wafer fab manufacturing location	*ANG MO KIO*
Wafer diameter	*6 inches*
Wafer thickness	*375 µm*
Silicon process technology	*BCDoffline*
Die finishing back side	*CHROMIUM/NICKEL/GOLD*
Die size	*1780X1780 µm*
Bond pad metallization layers	*AlSiCu*
Passivation	*NITRIDE*
Metal levels	*1*

Assembly Information	
Assembly plant location	*AMKOR ATP1-PHILIPPINES*
Package description	*SO16N*
Molding compound	*Sumitomo G600*
Wires bonding materials/diameters	*Au/1.2 mils*
Die attach material	*Ablestik 8290*
Lead solder material	*NiPdAu*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Revision
1	ABA
2	ACA
3	ACA
4	ACA with new LeadFrame Strip

4.2 Test plan and results summary

Die Oriented Tests (lot3=ADA–rotated die)							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1 (ABA)	Lot 2 (ACA)	Lot 3 (ADA)		
HTRB	High Temperature Reverse Bias						
		Tj=150°C, V_{HV}=630V, V_{TPR}=20V,V_{DD}=3.3V	0/40	--	--	1000h	
HTOL	High Temperature Operating Life						
	PC before	Tj=150°C V_{HV}=600V, V_{EOL}=4V,V_{DD}=5V, V_{CC}=16V	0/80	--	--	1280h	
	PC before	Tj=150°C V_{HV}=600V, V_{EOL}=4V,V_{DD}=5V, V_{CC}=16V	--	--	0/77 (*)	1000h	

	Package Oriented Tests (lot3=ADA–rotated die)							
Test	Method	Conditions	Failure/SS				Duration	Note
			Lot 1	Lot 2	Lot 3	Lot 4		
PC		Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	0/260	--	0/231	0/231		
SWS	Solder Wave Simulation	According Jedec 22-A11	Passed 100	--	Passed 77	--		
AC		Autoclave						
	PC before	121°C 2atm	0/110	--	0/77	--	168h	
AC		Autoclave						
	PC before	121°C 2atm	--	--	--	0/77	96h	
TC		Temperature Cycling						
	PC before	Temp. range: -65/+150°C	0/110	--	0/77	0/77	500cy	
HTSL		High Temperature Storage						
	No bias	Tamb=150°C	0/110	--	0/77	--	1280h	
HTSL		High Temperature Storage						
	No bias	Tamb=150°C	--	--	--	0/77	1000h	
THB		Temperature Humidity Bias						
	PC before	Ta=85°c/85%R.H, Tj=150°C V_{HV}=118V, VDD=3,3V, V_{TPR}=18V	0/40	--	--	--	1000h	

Electrical Characterization Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
ESD	Electro Static Discharge						
	Human Body Model	**+/- 2kV** **+/- 900V on HV pins**	--	**0/3**	**0/3**		
	Charge Device Model	**+/- 500V**	--	**0/3**	**0/3**		
LU	Latch-Up						
	Over-voltage and Current Injection	**Tamb=100°C** **Jedec78**	--	**0/6**	--		

(*) See detailed results on section 4.2.1

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr. and 1280hrs) @ Ta=25°C

(*) After 1000h a drift on Fosc_Funz parameter was observed: due to the drift some devices went out of spec.
In order to compensate the drift and to avoid out of spec., new trimming target value was defined in agreement with the customer.
On the basis of the above corrective action, we consider concluded the HTOL trial with 0 rej.

5.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168hrs and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.2.4 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 200 cycles.
- Final Testing @ 500 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -65°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.5 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-100mA	Inom+100mA	Vcc=16V
IN high: 3.3V	-100mA	Inom+100mA	Vcc=16V

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011

Reliability Qualification Report SO14 Leadframe Strip Change in Amkor (From HD to XD) - AMKOR PCN 140501

General Information	
Product Line	**0914**
Product From	**FBK7*0914AAW**
Package Technology	**K7 SO 14 .15 TO JEDEC MS-012**

Locations	
Wafer Fab Location	**AM6F - Singapore 6"**
Assembly Plant Location	**ZY1A SC AMKOR ATP1 - PHILIPPINES**
Testing Plant	**ZW1T SC AMKOR ATP3 - PHILIPPINES**
Reliability Assessment	**ZW1T SC AMKOR ATP3 - PHILIPPINES (QA RELIABILITY LAB)**

Issued By: Sandra KRIEF

Approved By: Jean-marc BUGNARD

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document Reference	Short Description
AEC-Q100	Stress test qualification for integrated circuits
SOP 2.6.11	Project management for product development
SOP 2.6.19	Front-end technology platform development & qualification
SOP 2.6.2	Internals change management
SOP 2.6.7	Product maturity level
SOP 2.6.9	Package and process maturity management in Back End
SOP 2.7.5	Automotive products definition and status
0061692	Reliability tests and criteria for product qualification
8160601	Internal reliability evaluation report template
8161393	General specification for product development

2 TEST GLOSSARY

TEST NAME	DESCRIPTION
PC (JL1)	Preconditioning (Solder Simulation)
TC	Temperature Cycling
AC or PPT	Autoclave or Pressure Pot Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The aim of this report is to present the results of the reliability assessment evaluation performed on TS914IDT$BAF (FBK7*0914AAW) – the Lead- frame strip changed in Assembly Plant AMKOR ATP1 – PHILIPPINES (from HD to XD), impact on package K7 SO 14 .15 TO JEDEC MS-012 (with reference to AMKOR PCN 140501).

The main purpose is to qualify XD Lead-frame as a new strip for K7 SO 14 .15 TO JEDEC MS-012.

TS914ID$BAF is processed in CMOS 3µm, C1PAHV-2 / 2 poly (14/1m), diffused in AM6F - Singapore 6" and assembled in AMKOR ATP1 – PHILIPPINES.

For the reliability assessment evaluation the following package oriented test were carried out:

Preconditioning JL1 (3X Reflow)
Temperature Cycling (TC)
Autoclave / Pressure Pot Test (AC / PPT)

3.2 Conclusions

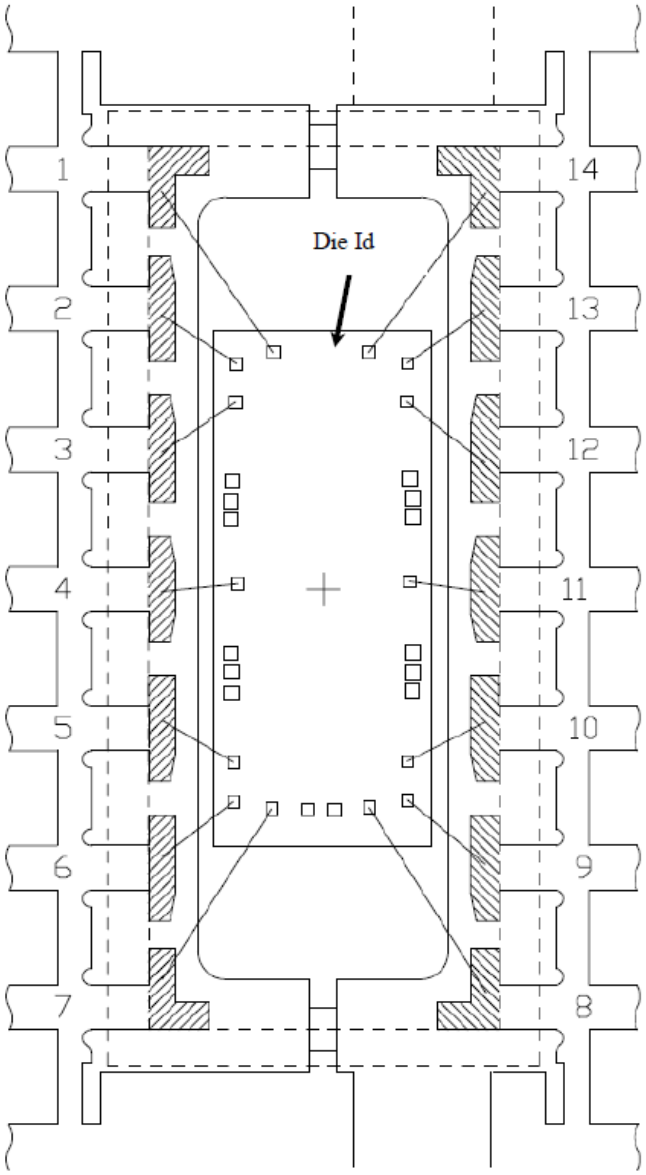
All reliability tests have been completed with positive results (no any electrical failure that can be link to new Lead-frame strip changed from HD to XD). Package oriented test and destructive physical analysis - SAM also have not put in evidence any criticality to package robustness.

4 DEVICE CHARACTERISTICS

4.1 Bond Diagram

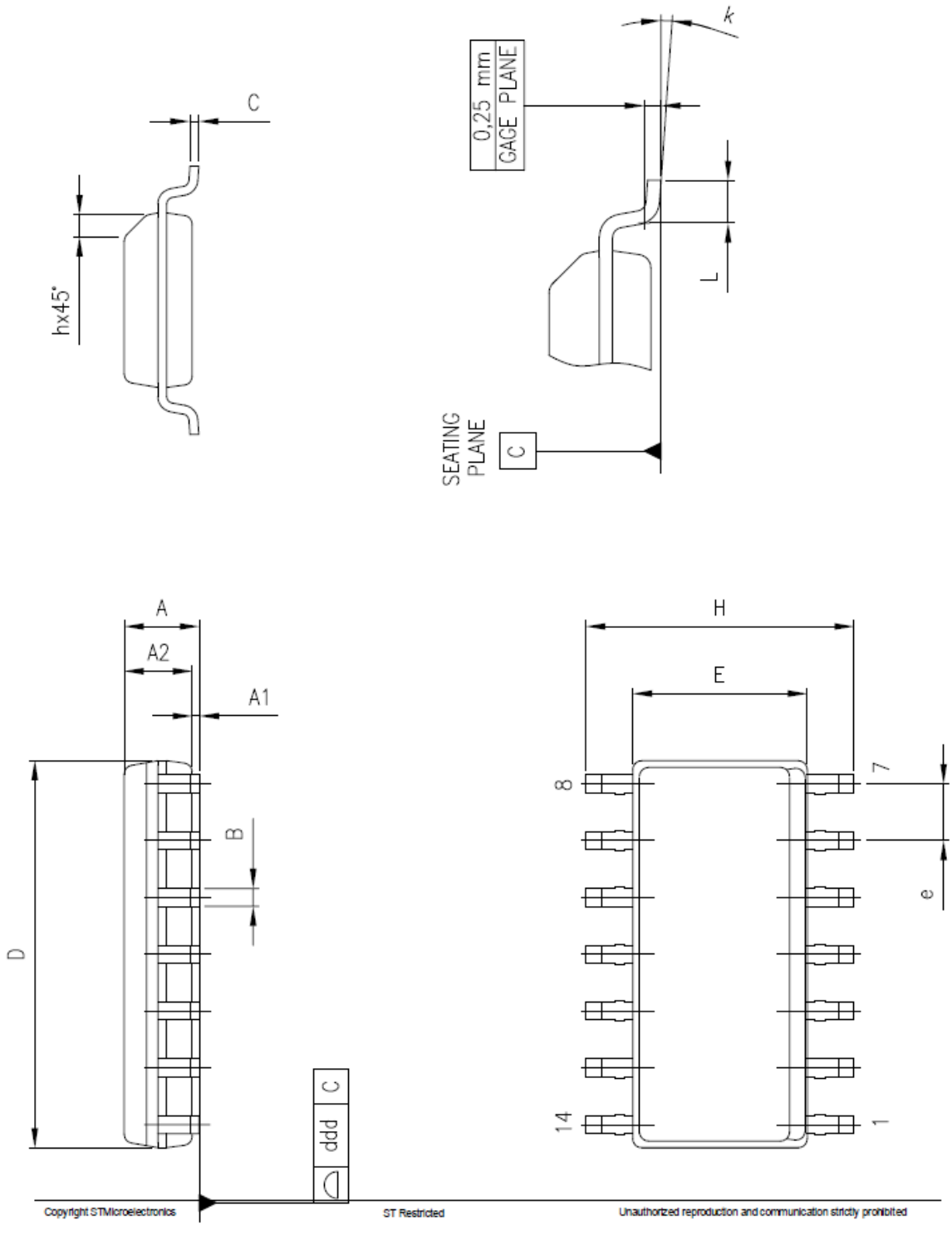
BONDING DIAGRAM FOR LINE: 0914 PACKAGE: K7

FRAME PAD : 0.090 x 0.280 inches
2.28 x 7.11 mm



SOP 14
BLANK BONDING DIAGRAM REFERENCE: 101317464

4.2 Package Outline / Mechanical Data



	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A	1.35		1.75			1.75	
A1	0.10		0.25	0.10	0.15	0.20	
A2	1.10		1.65	1.48	1.52	1.60	
B	0.33		0.51	0.35	0.40	0.455	
C	0.19		0.25	0.19	0.20	0.238	
D	8.55		8.75	8.60	8.65	8.70	(1)
E	3.80		4.00	3.80	3.90	4.00	
e		1.27			1.27		
H	5.80		6.20	5.90	6.00	6.10	
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	0.50	0.635	0.685	
k	0		8	2	4	8	DEGREES
ddd			0.10			0.04	

NOTES:

(1) – Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

(2) – Drawing dimensions include Single and Matrix versions.

4.3 Traceability

Wafer Fab Information	
Wafer fab manufacturing location	AM6F - Singapore 6"
Wafer diameter	6 inch
Wafer thickness (X0914AAW)	280+/-20 UM
Silicon process technology	CMOS 3µm - C1PAHV-2
Die finishing back side	RAW SILICON
Die finishing front side	P-VAPOX/NITRIDE
Die size	4650 x 1960µm

Assembly Information	
Assembly plant location	ZY1A SC AMKOR ATP1 - PHILIPPINES 9998
Package description	K7 SO 14 .15 TO JEDEC MS-012
Molding compound	SUMITOMO G600
Wire bonding materials/diameters	Au 1.0 Mils
Die attach material	ABLESTIK 8290
Lead frame material	LF SO E14L 90x280 XD SID 101385254 C194

Final Testing Information	
Electrical testing location	ST SINGAPORE EWS,SGEWS 0899
Tester	ASL1K

5. TEST RESULTS SUMMARY

5.1 Lot Information

Lot #	Diffusion Lot	Device name	AMKOR ID	ATF#
1	W532T59B	TS914ID$BAF	2862566	A3S1625LG0315

5.2 Test Plan and Results Summary (Electrical Test)

Reliability Test Status						
No	Test Name	Prec	Condition/ Method	Steps	Fails/SS	Notes
					Lot 1	
1	PC (JL1)		Bake 24hrs @ 125°C Soak 168hrs @ 85°C/85%RH 3 Reflow 260°C Profile = J-STD-020D	Final	0 / 200	Pass
2	TC	Yes	Test Conditions = -65°C / +150°C	500cyc	0 / 77	Pass
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 77	Pass

NOTES

All units electrically tested good (all Pass) after each reliability readout. No any electrical failure found that can be link to the weakness of the assembly process or due the Lead-Frame Strip change from HD to XD in Amkor Philippines (ATP1).

5.3 Test Plan and Results Summary (SAM Analysis)

Reliability Test Status						
No	Test Name	Prec	Condition/ Method	Steps	Fails/SS Lot 1	Notes
1	PC (JL1)		Bake 24hrs @ 125°C Soak 168hrs @ 85°C/85%RH 3 Reflow 260°C Profile = J-STD-020D	Final	0 / 44	No Delam
2	TC	Yes	Test Conditions = -65°C / +150°C	500cyc	0 / 22	No Delam
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 22	No Delam

NOTES

SAM analysis did not reveal any delam on Die Attach Material (DAM) & Die / Molding Compound (Die Top) on sampling basis 22 pcs for each reliability test The Lead and die-paddle delam (die-pad front side / molding compound) after Reliability (TC Trial) is an intrinsic problem of this package and not related to the change being qualified.

All units with or without Lead delam passed the electrical testing after TC500 and no lifted weld or broken weld during pull test after TC500.

6. TESTS DESCRIPTION

6.1 Package tests description

TEST NAME	DESCRIPTION	PURPOSE
PC (JL1) Preconditioning MSL1 (solder simulation)	**The device is submitted to a typical temperature profile used for surface mounting after storage in a control moisture absorption.**	**As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.**
TC Temperature Cycling	**The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.**	**To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are link to metal displacement, dielectric cracking, molding compound delamination, wire bonds failure, die crack.**
AC or PPT Autoclave / Pressure Pot Test	**The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature**	**To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.**