Reliability Report

Voltage Regulator

SO8L Pkg & New Bom Qualification

In Bouskoura Plant

T.V:L78L05CD13TR

Technology: Bipolare>6nm Ang Mo Kio

General Information	
Product Line	LA051
Product Description	5V 100Ma Pos Reg
P/N	L78l05CD13TR
Product Group	AMG
Product division	General Purpose Analog & RF Division Power Management
Packages	SO8
Silicon Process technology	BIPOLARE>6nm

Locations	
Wafer fab	*Ang Mo Kio*
Assembly plant	*Bouskoura*
Reliability Lab	*CATANIA*
Reliability assessment	*pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	May 2016	8	Angelo Basile	Giovanni Presti	Final report

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The present Reliability Evaluation is related to the New SO8 in HD line & New BOM Qualification in BSK for the Voltage Regulator & Vref BU (32)

Product process:

FE: **BIP111, LAAT, HBIP40**

The reliability verification will involve Test Vehicles coming from different FE processes, in order to cover, in a general way, the FE/BE compatibility.

BE: SO8 HD line & New BOM

- **SO8 HD Line: New Frame SO 8L 94x125 HD BTW 320u SpAg**
  (on behalf of SO 8L 94x125 HD OpA 320u SpAg – Sumitomo - PCN IPG-IPC/14/8322)
- **New BOM: Molding Compound SUMITOMO EME G700KC**
  (on behalf of SUMITOMO EME-G630AY)
- **Wire: Cu 1.0 mils**

Industrial Domain:

Automotive (JL3, AEC - Q100)
Industrial (JL1, JESD47)

3.2 Evaluation Plan

Taking in consideration the industrial domain and FE technology, we will have:

- **Automotive**
  - o 0431AI6 BIP111,
  - o 1431AE6 BIP111,

- **Industrial**
  - o LA05AA6 LAAT, 1 metal AlSi da 3 um, passivazione Nitride, no backmetal
  - o LA17AB6 LAAT, 1 metal AlSi da 3 um, passivazione Nitride, no backmetal

  - o 0431BB6 HBIP40, 1 metal AlSiCu da 1.45 um, PVAPOX+Nitride, no backmetal
  - o M413AC6 HBIP40, 1 metal AlSiCu da 1.45 um, PVAPOX+Nitride+PIX, no backmetal

The plan will involve the following Test Vehicles/lots number.

	Test Vehicles		Technology	Lot number	Jedec Level	Reference spec.
	Line	Product				
Automotive	0431AI6	TL431AIYDT	BIP111	1 Lot	JL3	AEC - Q100
	1431AE6	TL1431AIYDT		2 Lots	JL3	AEC - Q100
STD Products	LA05AA6	L78L05ABDTR	LAAT	1 Lot by TV	JL1	JESD47
	0431BB6	TL431CDT	HBIP40	1 Lot by TV	JL1	JESD47
Total lot number				5 Lots		

The Full Rreliability Evaluation Plan will follow:

- The AEC-Q100 for the Automotive Grade Products
- The JESD47 for the STD ICs Products

The present Report is related to the Test Vehicle L78LA05ABDTR.

3.3 Conclusion

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Qualification Plan requirements have been fulfilled without exception with reference to TL431CDT. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime

The evaluation plan will be completed as the other TVs (minimum 3 assembly Lots) will complete the reliability evaluation.

4 DEVICE CHARACTERISTICS

4.1 Device description

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The L78L series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat-sink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or oncard regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The L78L series used as Zener diode/resistor combination replacement, offers e improvement along with lower quiescent current and lower noise.

4.2 Construction note

P/N	L78L05CD13TR
Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio
Technology	Bipolar.6nm
Die finishing back side	Lapped Silicon
Die size	1130 x 1270 micron
Passivation type	SiN (NITRIDE)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ASL1000
Test program	LA05QAE01
Assembly information	
Assembly site	Bouskoura
Package description	SO 08 .15 Jedec
Molding compound	SUMITOMO EME-G700KC
Frame material	SO 8L 94x125 Mtx HD OpM 320u SpAg
Die attach material	Glue Loctite Ablestik 8601S-25 10cc/18g
Wires bonding materials/diameters	Cu Wire 1 mils
Final testing information	
Testing location	Bouskoura
Tester	ASL1000
Test program	L78L05A-CD.prg

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	V6525XX5	CZ6030FR01	*PKO7*LA05AA6*	SO8L	LA0501	

5.2 Test plan and results summary

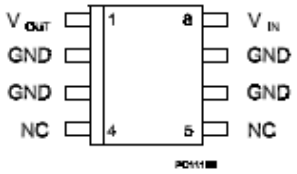
P/N L78L05CD13TR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
						SO8L	
Die Oriented Tests							
HTB	N	JESD22 A-108	Ta = 125°C, Vbias= +30V	77	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 H	0/45	
					500 H	0/45	
					1000 H	0/45	
HTSL	N	JESD22 A-103	Ta = 175°C	45	168 H	0/45	Eng Eval
					500 H	0/45	
					1000 H	0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times	231	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	168h	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH=85%, Vbias=+25V	77	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
Other Tests							
ESD		ANSI/ESD A JEDEC JS-002	CDM	3	+/-500V	Pass	

6 ANNEXES

6.1 Device details

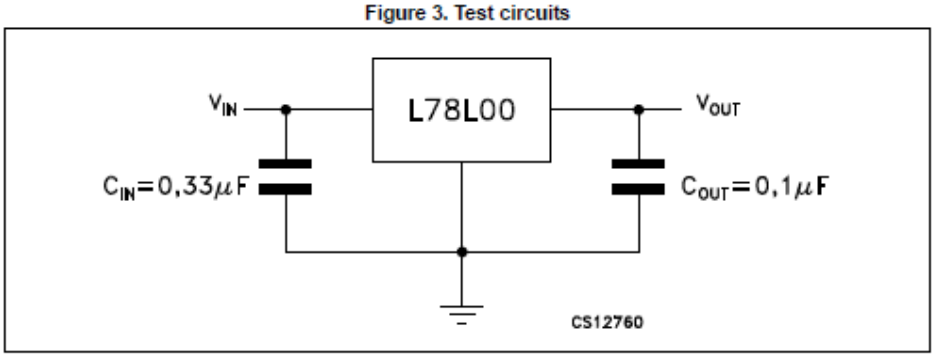
6.1.1 Pin connection



SO-8

6.1.2 Block diagram

Figure 3. Test circuits



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Test		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM**: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.