Public Products List

PCN Title : Voltage Reference: SOT23-3L Package Additional Assembly and Testing Plant in subcontractor Nantong FUJITSU (NFME China) for TS2431AILT, TS2431BILT and TS2431ILT

PCN Reference : AMG/16/9865

PCN Created on : 28-Jun-2016

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TS2431ILT	TS2431AILT	TS2431BILT

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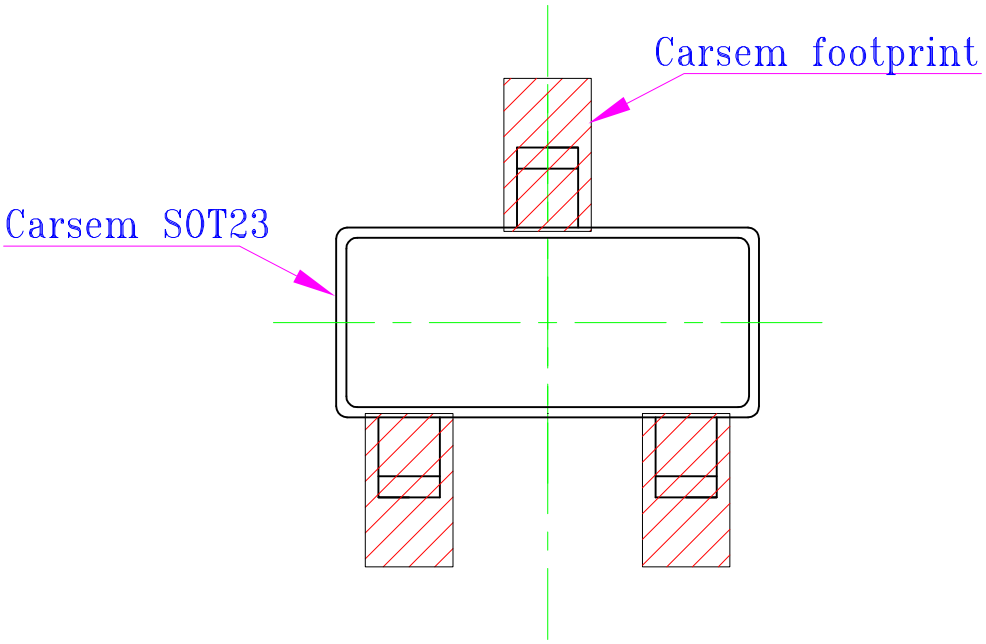
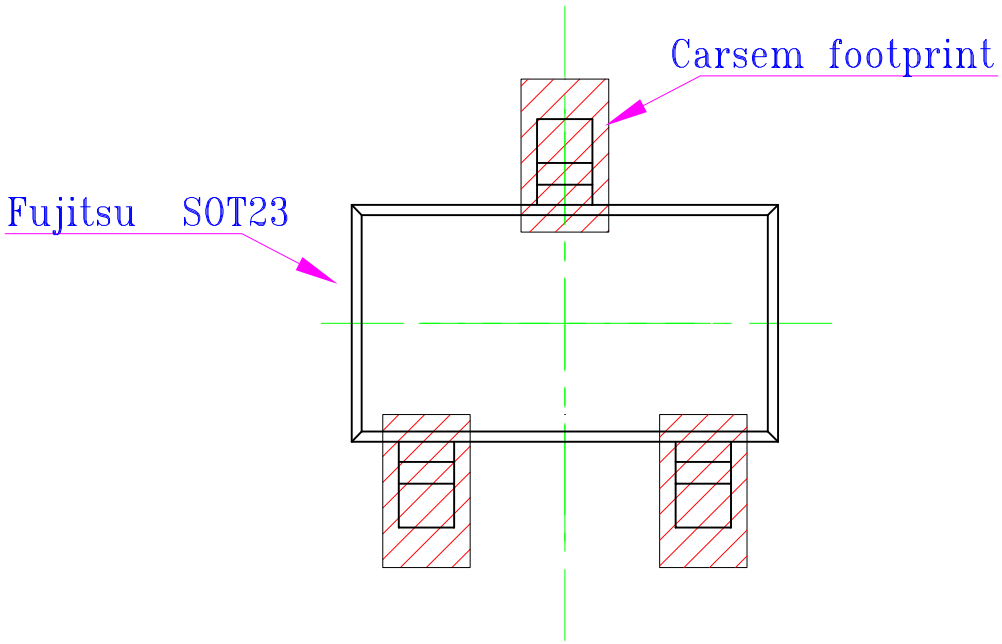
Overlapped Carsem footprint with SOT 23 packages

SOT 23 3L Carsem



SOT 23 3L Fujtsu



Reliability Report

New Package Qualification

Package: SOT23 3L assembled in NFME Plant

T.V.:TS2431AILT

General Information	
Product Line	U78201
Product Description	Programmable shunt voltage reference
P/N	TS2431AILT
Product Group	IPD.
Product division	General Purpose Analog & RF Power Management
Packages	SOT23 3L
Silicon Process technology	BICD2S

Locations	
Wafer fab	SINGAPORE Ang Mo Kio
Assembly plant	*SOT23-3L NFME*
Reliability Lab	*CATANIA*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	May-2016	7	Angelo Basile	Giovanni Presti	Final report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
PCB	Print Circuit Board

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the SOT23 3L package in NFME Subcontractor.
TV: TS2431AILT

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products.

4 DEVICE CHARACTERISTICS

4.1 Device description

The TS2431 is a programmable shunt voltage-reference with guaranteed temperature stability over the entire temperature range of operation - 40 to + 105 °C. The output voltage may be set to any value between 2.5 and 24 V with an external resistor bridge Available in a SOT23-3L surface mount package, the device can be implemented in applications where space-saving is of utmost importance.

4.2 Construction note

	P/N TS2431AILT
Wafer/Die fab. information	
Wafer fab manufacturing location	SINGAPORE Ang Mo Kio
Technology	BCD2S
Die finishing back side	LAPPED SILICON
Die size	1420 X 760 micron
Passivation type	PSG+Silicon Nitride+Polyimide
Wafer Testing (EWS) information	
Electrical testing manufacturing location	SINGAPORE Ang Mo Kio
Tester	ASL1000
Test program	TU782W 02
Assembly information	
Assembly site	NANTONG FUJITSU
Package description	SOT 23 3L
Molding compound	HITACHI CEL8240HF
Frame material	SOT23-3A 1.52X1.21
Die attach material	ABLE000018 8008MD WBC
Wires bonding materials/diameters	Au 1mils
Final testing information	
Testing location	NANTONG FUJITSU
Tester	ASL1000
Test program	TS2431 FT1.pgs

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	SOT23 3L	U78201	
2			
3			

5.2 Test plan and results summary

P/N TS243AILT

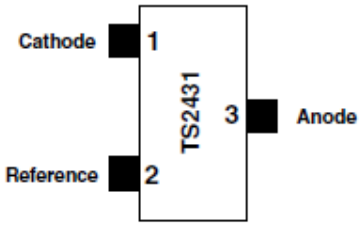
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						1st LOT	2nd LOT	3rd LOT	
Die Oriented Tests									
HTOL1 (*)	N	JESD22 A-108	Tj = 125°C, Vbias=+6V		168 H	0/77			Applicative Configuration
					500 H	0/77			
					1000 H	0/77			
HTOL2 (*)	N	JESD22 A-108	Tj = 125°C, Vbias=+25V		168 H	0/77	0/77	0/77	Ioff Configuration, AMR
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTSL (*)	N	JESD22 A-103	Ta = 150°C		168 H	0/25	0/25	0/25	
					500 H	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	
Package Oriented Tests									
PC (*)		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H	0/25	0/25	0/25	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	0/25	0/25	
					200 cy	0/25	0/25	0/25	
					500 cy	0/25	0/25	0/25	
THB1	Y	JESD22 A-101	Ta = 85°C Rh=85% Vbias=+6V		168 H	0/25	0/25	0/25	Applicative Configuration
					500 H	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	
THB2	Y	JESD22 A-101	Ta = 85°C Rh=85% Vbias=+20V		168 H	0/25	0/25	0/25	Ioff Configuration, AMR
					500 H	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	
(*) All the parts have been soldered on dedicated PCB									
Additional Test									
ESD	N	ANSI/ESDA/JEDEC JS-002	CDM @+/-1500V	3	Final	Pass			

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

Pin connections (top view)



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. and/or the absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.