



Public Products List

PCN Title : VIPower M0L7: Activation of Singapore 8" (AMK8) as additional location beside Catania 8" (CT8)

PCN Reference : ADG/16/9987

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Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

VN7040ASTR	VND7050AJ12TR	VND7140AJ12TR
VND7140AJTR	VND7020AJTR	VND7050AJTR
VN7016AJTR	VN7040AJTR	



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VIPOWER M0L7: Activation of Singapore 8" (AMK8) as additional location beside Catania 8" (CT8)

WHAT:

Please be informed that we have completed the activities to qualify AMK8 as additional location beside Catania 8" (CT8) for VIPOWER M0L7 products.

WHY:

Double Source, Capacity increase and service Improvement.

WHO:

See list of products involved

WHEN:

Change will be implemented from end of April 2017 upon Customer Agreement

Samples are available on demand

Qualification report included in this communication (RR002716CT2235)

WHERE:

ST Singapore 8" wafer fab (AMK8)

VIPower M0L7 Technology

Ang Mo Kio SG8 (Singapore) 8 inch Wafer Fab second source qualification

Revision history

Rev.	Date of Release	Author	Changes description
1.0	September 28, 2016	A. Vilardo - APG Q&R Catania	Creation

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- 1. Reliability evaluations overview

1.1 Objectives

Aim of this report is to present the results of the reliability evaluation performed on selected test vehicles designed in VIPower M0L7 Technology to qualify the ST SG8 Ang Mo Kio (Singapore) 8" Wafer Fab as second source for the mentioned silicon Technology products manufacturing.

These are single and double channels High-side drivers with Multi Sense analog feedback products for Automotive Applications assembled in SO8 and PSSO16 package.

Here below the chosen test vehicles:

Test vehicles general information			
Commercial Product	VN7040AS	VND7050AJ	VND7020AJ
Product Line	XV14	XV17	VNY6
Package	SO8	PSSO16	PSSO16

The qualification has been performed according to **Grade 1** of the **AEC_Q100 Rev.H** specification following the path described here below:

Test group as per AEC-Q100 Rev.H		Performed (Y/N)	Comment
A	Accelerated Environment Stress	Y	
B	Accelerated Lifetime Simulation	Y	
C	Package Assembly Integrity	Y	
D	Die Fabrication Reliability	Y	
E	Electrical Verification	Y	
F	Defect Screening	N	To be implemented starting from first production lot
G	Cavity Package Integrity	N	Not applicable

See details per each test group in section 3 of this report.

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In the below table a comparison between the AEC-Q100 and ZVEI requirements vs the applied ST qualification plan is reported:

	Test Group A				Test Group B			Test Group C			Test Group D					Test Group E						
	THB	AC	TC	PTC	HTSL	HTOL	ELFR	WBS	WBP	SD	PD	EM	TDDB	HCI	NBTI	SM	HBM	CDM	LU	ED	EMC	SC
AEC-Q100	x	x	x	x		x	x	x	x			x	x	x	x	x	x	x	x	x		
ZVEI	x	x	x	x		x	x	x	x			x	x	x	x	x	x	x	x	x		
ST	x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	x	x		

No deviation between AEC-Q100 / ZVEI requirements and ST qualification plan

1.2 Results

All reliability tests have been completed with positive results, neither functional nor parametric rejects were detected at final electrical testing.

The drift analysis showed a good stability for all the electrical parameters.

The Wire Bond Pull/Shear tests (WBP, WBS) as Package Assembly Integrity (test Group C) performed before and after the package oriented stress test pointed out neither abnormal break loads nor forbidden failure modes.

An extended reliability (2x AEC-Q100 requirement) trough selected stress test has been completed with positive results, also in this case neither functional nor parametric rejects were detected at final electrical testing.

Based on the overall positive results we consider the product AEC-Q100 Grade 1 qualified from a reliability point of view.

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- 2. Traceability

	VN7040AS	VND7050AJ	VND7020AJ
Wafer Fab Information			
Silicon process technology	VIPower M0L7		
Wafer fab manufacturing location	ST SG8 Ang Mo Kio (Singapore)		
Wafer diameter (inches)	8		
Die finishing back side	Ti-NiV-Au		
Die size (mm ²)	2500x1530	2800x1930	4050x2140
Metal levels / materials	2 Ti/TiN/Ti/AlCu/TiN (3.18 last)		
Die finishing front side	Teos + PTeos + SiOn + PIX		
Diffusion Lots #	VC602F7L	VC551F18	VC5085TP
Assembly Information			
Package description	SO8	PSSO16	
Assembly plant location	ST SHENZHEN (China)	ST SHENZHEN (China)	ST BOUSKOURA (Morocco)
Wires bonding material/diameter	CU 1mils, Cu 2 mils	CU 1mils, CU 2.5 mils	
Molding compound	SUMITOMO EME-G700KC	SUMITOMO EME-G700LS	
Die attach material	GLUE LOCTITE ABLESTIK QMI9507	PREFORM Pb/Ag/Sn 95.5/2.5/2	
Assembly Lot#	GK6171MV01	GK6140L901	CZ6160C5
Reliability Information			
Reliability test execution location	ST Catania (Italy)		

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- 3. Reliability qualification plan and results

Test group A: Accelerated Environment Stress					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
A1	PC Pre Cond	- Preconditioning according to Jedec JESD22-A113F including 5 Temperature Cycling Ta=-40°C/+60°C - Reflow according to level 3 Jedec JSTD020E - 100 Temperature Cycling Ta=-50°C/+150°C	Before THB, AC, TC, PTC, HTOL Reliability performed with units soldered on PCB		
A2	THB Temp Humidity Bias	Ta=85°C, RH=85%, Vcc=24V for 1000 hours	77/3	0/77/3	1 Lot/vehicle PTC only on VND7020AJ
A3	AC Autoclave	ENV. SEQ. Environmental Sequence TC (Ta=-65°C / +150°C for 100 cycles) + AC (Ta=121°C, Pa=2atm for 96 hours)	77/3	0/77/3	
A4	TC Temp. Cycling	Ta=-65°C / +150°C for 500 cycles	77/3	0/77/3	
A5	PTC Power Temp. Cycling	Ta=-40°C / +125°C for 1000 cycles Incandescent lamps loads 2xP27W+R5W each channel, ton=10ms, toff=30s, 120K activations within 1000cy	45/1	0/45/1	
A6	HTSL High Temp. Storage Life	Ta=150°C for 1000 hours.	45/3	0/45/3	

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Test group B: Accelerated Lifetime Simulation					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
B1	HTOL High Temp. Op. Life	Bias Dynamic stress OLT (JESD22-A108) Tj=150°C, PWM=100Hz, D.C.=68%, 1000 hours. Duration according to Mission Profile based on Ea=0.7eV	80/3 1 Lot/vehicle 40pcs/channel used on dual channels	0/80/3	Used Load: VN7040AS: P27W+R5W lamps VND7050AJ: P27W lamps VND7050AJ: 2xP27W+R5W lamps
B1	HTOL High Temp. Op. Life	Bias Static stress HTRB (JESD22-A108) Ta=125°C for 1000 hours	77/3	0/77/3	1 Lot/vehicle
B2	ELFR Early Life Failure Rate	Parts submitted to HTOL per JESD22-A108 requirements; GRADE 1: 24 hours at 150°C	800/3	No fail	1 Lot/vehicle
B3	EDR Endurance Data Retention	Only for memory devices	-	-	Not Applicable

Test group C: Package Assembly Integrity					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
C1	WBS Wire Bond Shear		30 bonds /minimum 5 units/3 lots	All measurement within spec limits	1 Lot/vehicle
C2	WBP Wire Bond Pull		30 bonds /minimum 5 units/3 lots	All measurement within spec limits	
C3	SD Solderability		-	-	Not Applicable
C4	PD Physical Dimensions		-	-	Not Applicable
C5	SBS Solder Ball Shear	Only for BGA package	-	-	Not Applicable
C6	LI Lead Integrity	Not required for Surface Mount Devices	-	-	Not Applicable

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Test group D: Die Fabrication Reliability					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
D1	EM Electromigration			Done	
D2	TDDB Time Dependent Dielectric Breakdown			Done	
D3	HCI Hot Carrier Injection			Done	
D4	NBTI Negative Bias Temperature Instability			Done	
D5	SM Stress Migration			Done	

Test group E: Electrical Verification					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
E2	ESD HBM		3 lots	Output, Input, SEn, SELx, VCC, FR_Stby: ±4.0kV MultiSense: ±2.0kV	1 Lot/vehicle
E3	ESD CDM		3 lots	±750V	1 Lot/vehicle
E4	LU Latch-Up		6/3	Inj-Low/Inj-High @ 25°C and 125°C: ±100mA all pins Inj+Low/Inj+High @ 25°C and 125°C: ±100mA all pins Overvoltage: passed	1 Lot/vehicle
E5	ED Electrical Distributions		30/3	Done	1 Lot/vehicle
E9	EMC Electromagnetic Compatibility		-	-	Not Applicable
E10	SC Short Circuit Characterization	According to AEC-Q100-012	-	Not Applicable	

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Test group F: Defects Screening Tests					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
F1	PAT Process Average Testing				Not performed on qualification lots listed on traceability section of this report. To be implemented starting from first production lot
F2	SBA Statistical Bin/Yield Analysis				

Test group G: Cavity Package Integrity Tests					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
G1	MS Mechanical Shock				Not applicable: not for plastic packaged devices
G2	VFV Variable Frequency Vibration				
G3	CA Constant Acceleration				
G4	GFL Gross/Fine Leak				
G5	DROP Package Drop				
G6	LT Lid Torque				
G7	DS Die Shear				
G8	IWV Internal Water Vapor				

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- 4. Extended reliability results (2x AEC-Q100)

AEC #	Test Name	STM Test Conditions	Sample Size/Lots	Results Fails/SS/Lots	Comments
A2	THB Temp Humidity Bias	Ta=85°C, RH=85%, Vcc=24V for 2000 hours	77/3	0/77/3	1 Lot/vehicle
A4	TC Temp. Cycling	Ta=-65°C / +150°C for 1000 cycles	67/3	0/67/3	
A6	HTSL High Temp. Storage Life	Ta=150°C for 2000 hours	35/3	0/35/3	
B1	HTOL High Temp. Op. Life	Bias Dynamic stress OLT (JESD22-A108) Tj=150°C for 2000 hours	77/3	0/77/3	
B1	HTOL High Temp. Op. Life	Bias Static stress HTRB (JESD22-A108) Ta=125°C for 2000 hours	77/3	0/77/3	

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