Dear Customer,

Following the continuous improvement of our service and in order to increase Power MOSFET productivity, this document is announcing that MDmesh™ K5 Technology devices, currently manufactured in Catania Wafer fab, will be also produced in Ang Mo Kio (Singapore) Wafer Fab.

MDmesh™ K5 Technology products manufactured in Ang Mo Kio (Singapore), guarantees the same quality and electrical characteristics as reported in the relevant data sheet. Devices used for qualification are available as Samples.

The involved product series and affected packages are listed in the table below:

Product Family	Technology	Commercial Product / Series
Power MOSFET Transistors	MDmesh™ K5	See attached list

Any other Product related to the above series, manufactured in the ST's Ang Mo Kio (Singapore) FAB, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program results and plan:

The reliability test report and plan are provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available as per table below.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle	Sample availability	1st Shipments
Power MOSFET Transistors	TO-220 IPAK	STP20N95K5 STU6N95K5	week 10-2015	From week 23-2015

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of MDmesh™ K5 Technology devices, produced in ST's Ang Mo Kio (Singapore) FAB, will be ensured by traceability code.

Sincerely Yours.

Reliability Report

MDmesh™ K5 Technology Front-End Capacity Extension - Ang Mo Kio (Singapore)

General Information	
Product Lines:	VJLL01 VJL301
Product Families:	Power Transistor
P/Ns:	STP20N95K5 STU6N95K5
Product Group:	IPG
Product division:	Power Transistor Division
Package:	TO-220 IPAK
Silicon Process techn.:	MDmesh™ K5

Locations	
Wafer Diffusion Plants:	Ang Mo Kio (Singapore)
EWS Plants:	Ang Mo Kio (Singapore)
Assembly and testing plant:	ST Shenzhen (China)
Reliability Lab:	*IPG-PTD Catania Reliability Lab. (Italy)*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	March 2015	7	A. Settinieri	C. Cappello	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for MDmesh™ K5 Technology Front-End Capacity Extension - Ang Mo Kio (Singapore).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel HV Power MOSFET

4.2 Construction note

Lot 1-2 D.U.T.: STP20N95K5 LINE: VJLL PACKAGE: TO-220

Wafer/Die fab. Information IGBT	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	MDmesh™ K5
Die finishing back side	Ti/Ni/Ag
Die size	6830 x 5060 µm²
Metal	AlSi
Passivation type	Teos + Nitride
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-220
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Gate: Al – Mg; Source: Ribbon Al
Lead finishing	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTest

Lot 3 D.U.T.: STU6N95K5 LINE: VJL3 PACKAGE: IPAK

Wafer/Die fab. Information IGBT	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	MDmesh™ K5
Die finishing back side	Ti/Ni/Ag
Die size	3950 x 2910 µm²
Metal	AlSi
Passivation type	Teos + Nitride
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	IPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Gate: Al – Mg; Source: Al
Lead finishing	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTest

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STP 20N95K5	VJLL01	N-channel HV Power MOSFET
2			
3	STU6N95K5	VJL301	

5.2 Reliability test plan summary

Test	Std ref.	Conditions	SS	Steps	Failure/SS		
					Lot 1	Lot 2	Lot 3
Die Oriented Tests							
TEST		All qualification parts tested per the requirements of the appropriate device spec.			235	235	235
External Visual		All devices submitted for testing			235	235	235
HTRB	JESD22 A-108	TA =150°C, BIAS=760V	135	168 H	0/45	0/45	0/45
				500 H	0/45	0/45	0/45
				1000 H	0/45	0/45	0/45
HTFB	JESD22 A-108	TA= 150°C, BIAS = 30V	135	168 H	0/45	0/45	0/45
				500 H	0/45	0/45	0/45
				1000 H	0/45	0/45	0/45
HTSL	JESD22 A-103	TA= 150°C	135	168 H	0/45	0/45	0/45
				500 H	0/45	0/45	0/45
				1000 H	0/45	0/45	0/45
Package Oriented Test							
AC	JESD22 A-102	Pa=2Atm / TA=121°C	75	96 H	0/25	0/25	0/25
TC	JESD22 A-104	TA= -65°C to 150°C	75	100 cy	0/25	0/25	0/25
				200 cy	0/25	0/25	0/25
				500 cy	0/25	0/25	0/25
H3TRB	JESD22 A-101	TA=85°C , RH=85%, BIAS= 100V	75	168 H	0/25	0/25	0/25
				500 H	0/25	0/25	0/25
				1000 H	0/25	0/25	0/25
IOL / TF	MIL-STD-750 Method 1037	ΔTC=105°C	75	10Kcy	0/25	0/25	0/25

6 ANNEXES 6.0

6.1 Tests Description

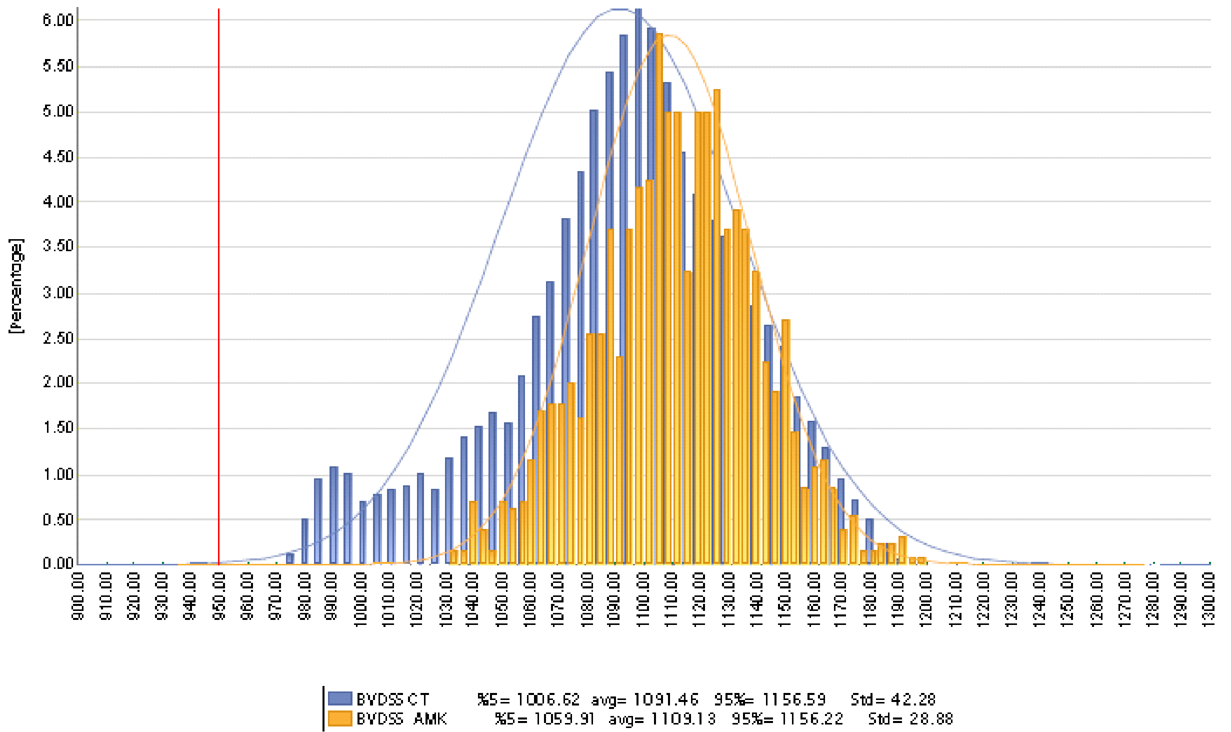
Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

VJL3 e VJLL:
Catania vs Ang Mo Kio

life.augmented

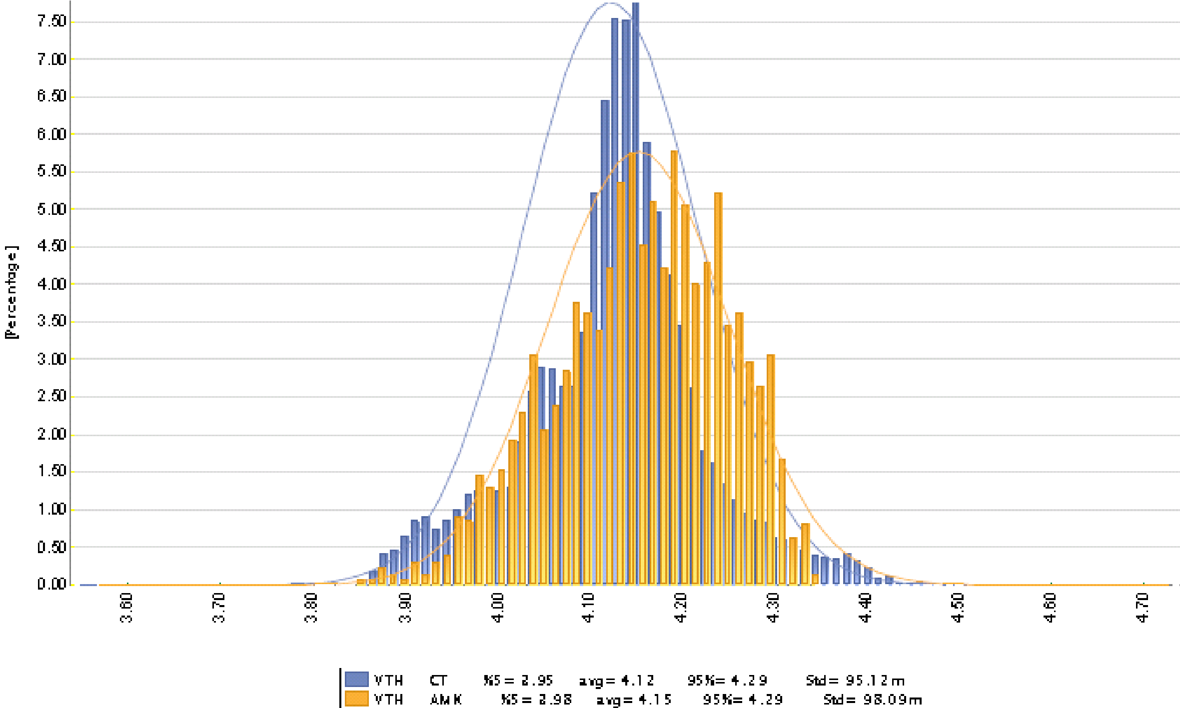
BVDSS@1mA

VJL3



Vth@100uA

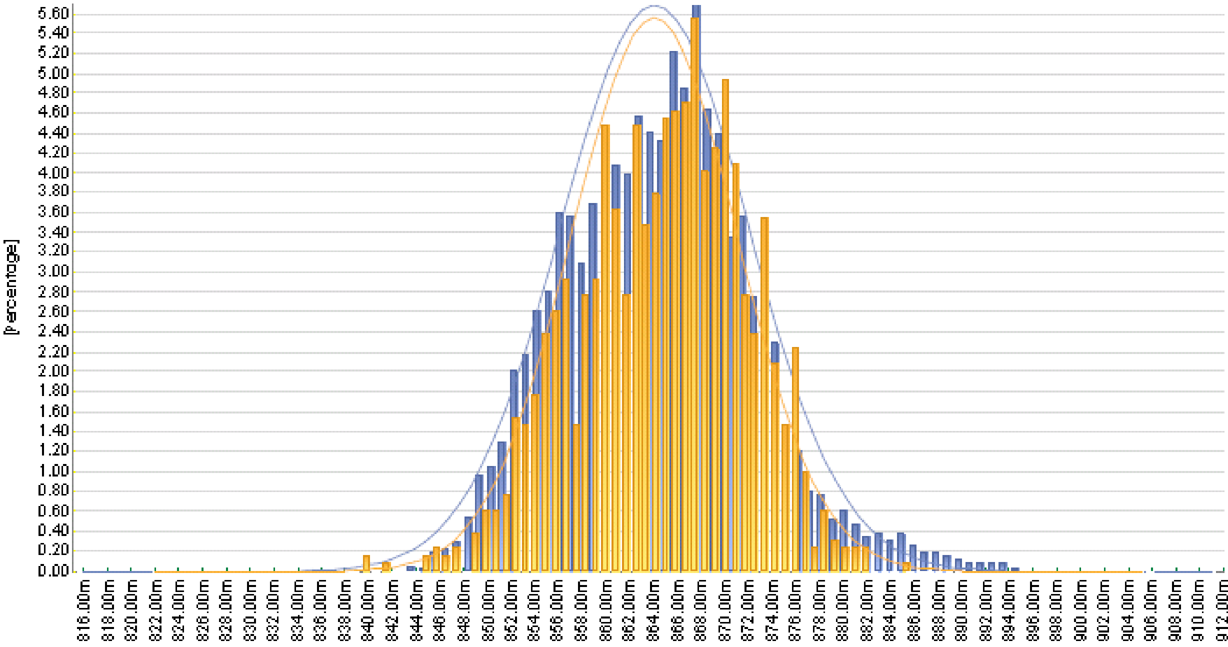
VJL3



life.augmented

RDSon@3A

VJL3



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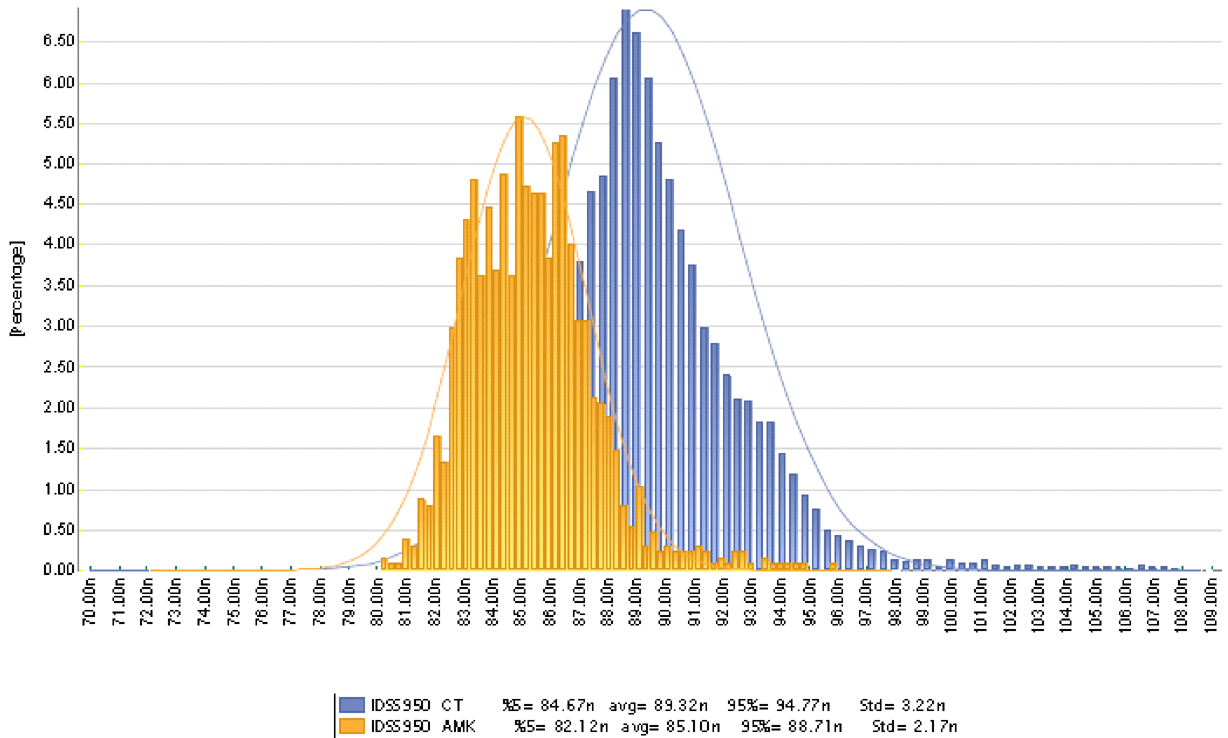
VJL3

VJL301

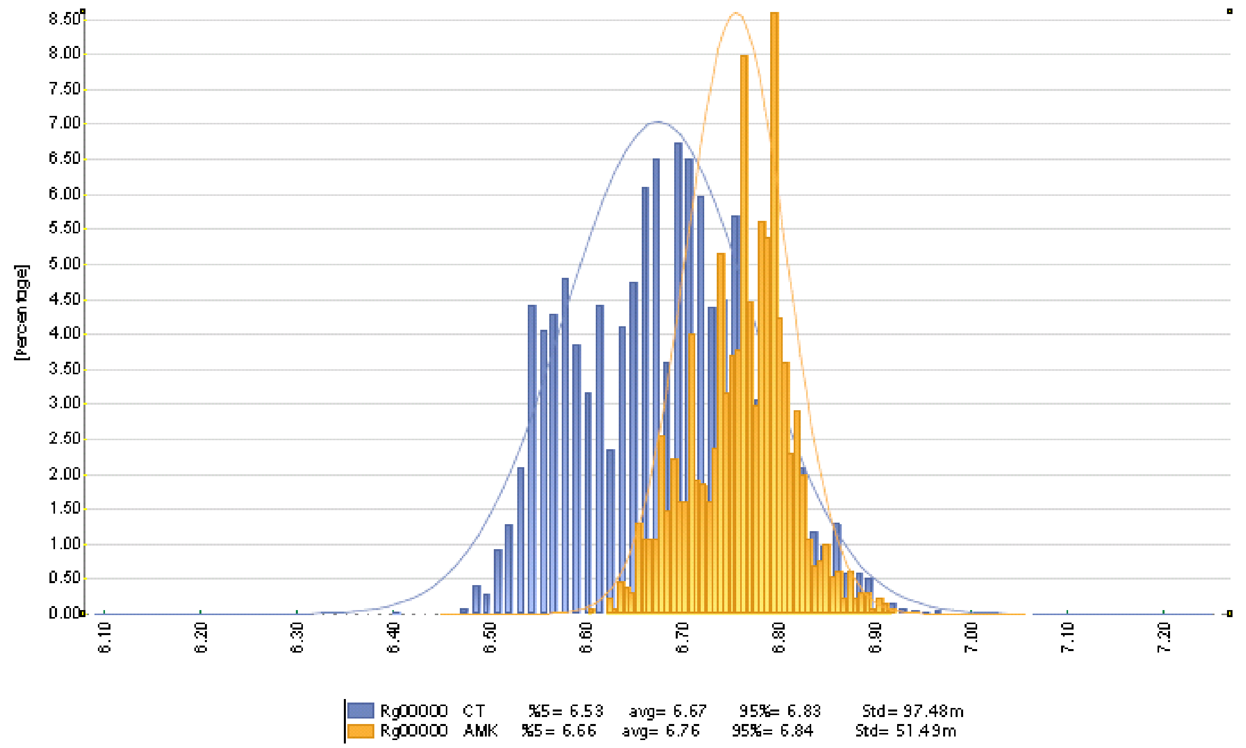


Rg

VJL3

QuickGraph v4.9

VJL301



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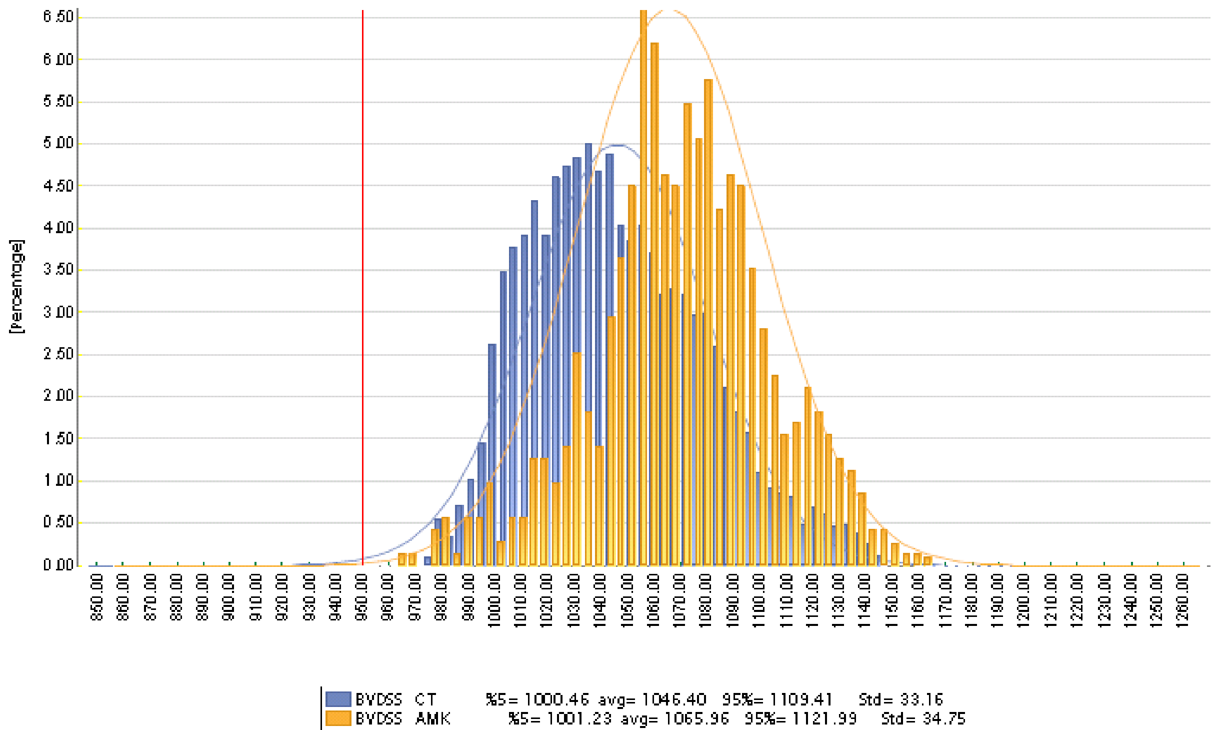
VJLL

Quick Graphic 4.3

VJLL01



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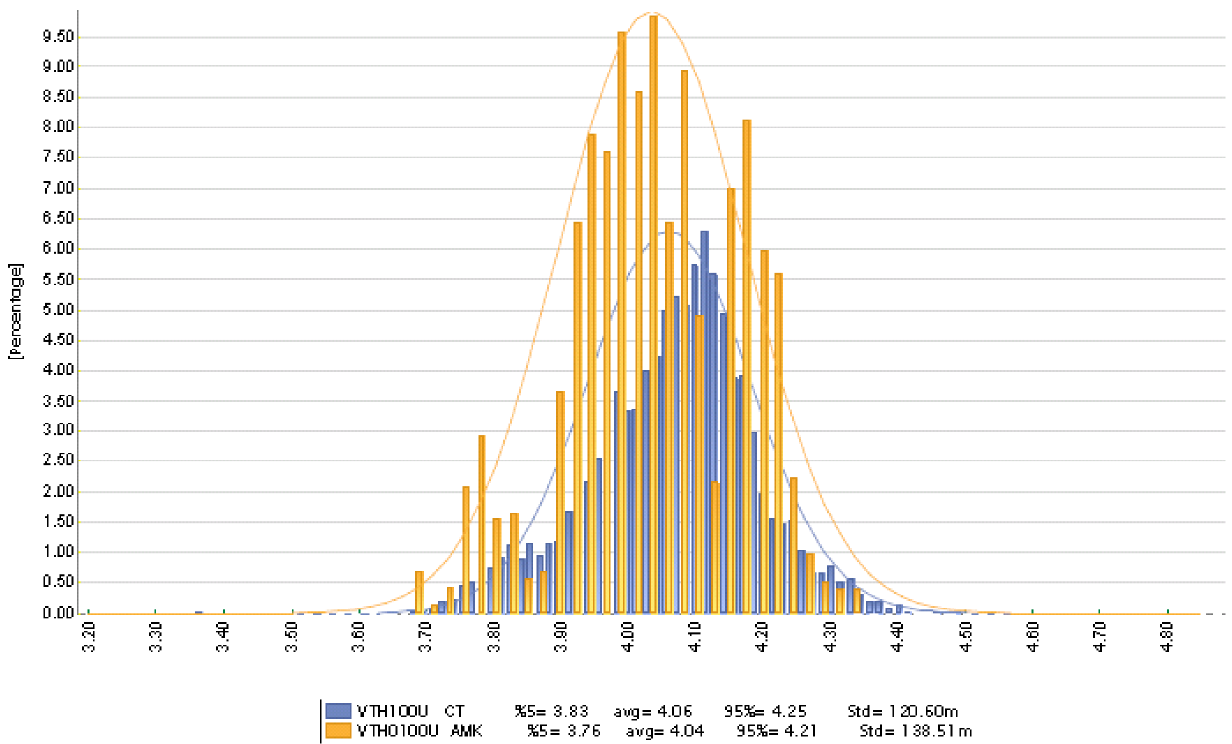
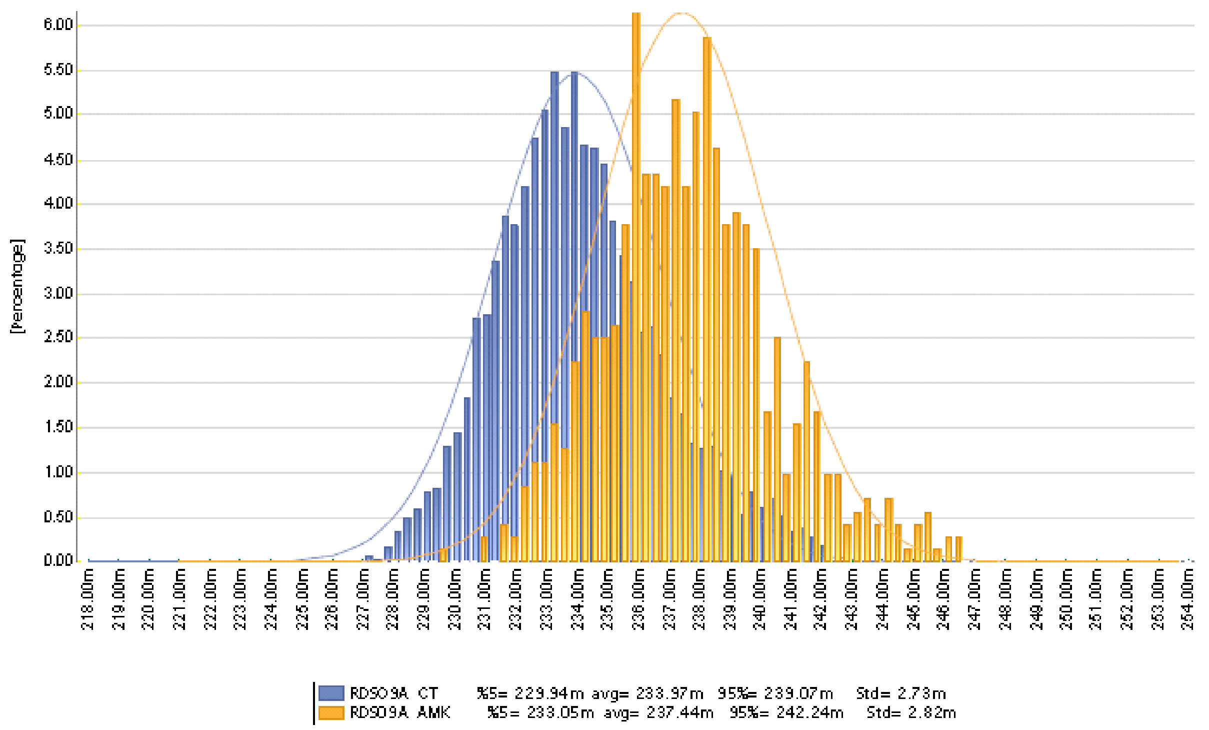
VJLL



life.augmented

RDSon@9A

VJLL



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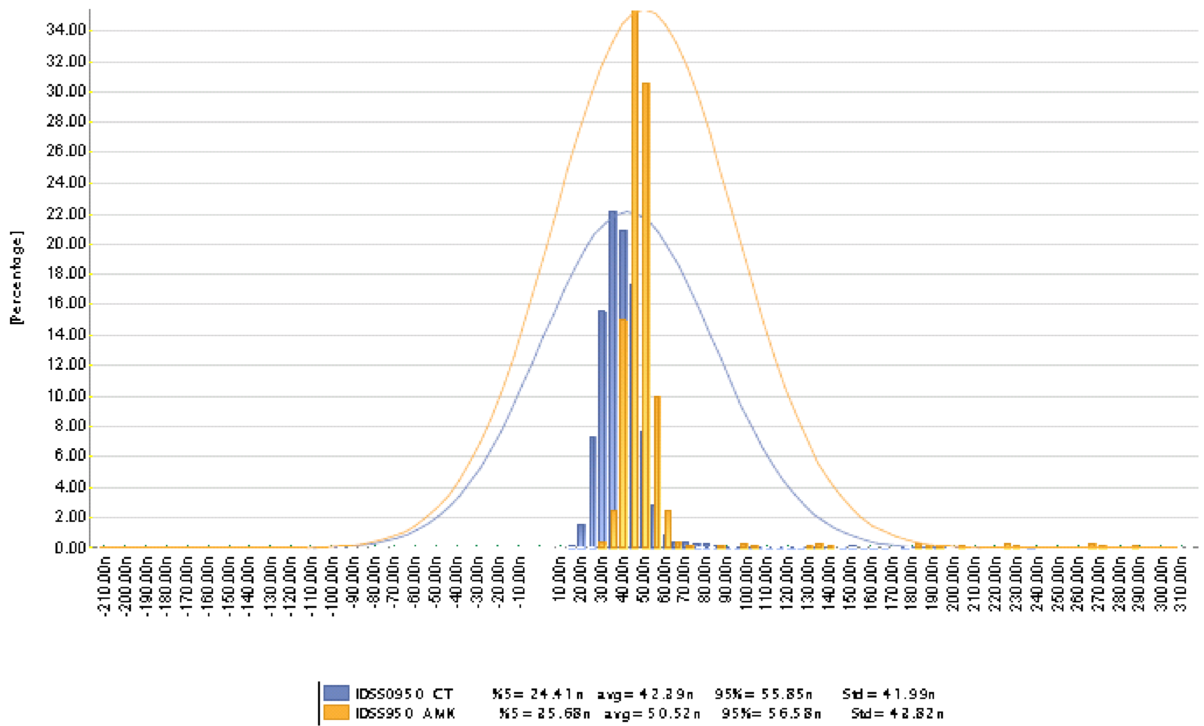
VJLL

VJLL01



life.augmented

Rg
VJLL