STMicroelectronics
ADG - ASD & IPAD™ Division[1]
BU Protection & IPAD

(1) ADG: Automotive and Discrete Group - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

PCN
Product/Process Change Notification

Qualification of a new assembly and test line at subco in China

Notification number:	ADG-DIS/18/10834	**Issue Date**	05/04/2018
Issued by	Aline AUGIS		
Product series affected by the change		SMB package • VRM <= 33 V, VBR <= 39 V • SM6T6V8A / CA to SM6T39A / CA • SMBJ5.0A / CA to SMBJ33A / CA	
Type of change		New assembly line for extra capacity	

Description of the change

STMicroelectronics is qualifying a new assembly line of SMB package subcontracted in China.

Reason for change

STMicroelectronics has decided to expand the manufacturing capacity of TVS protection devices housed in SMB package. This additional assembly line is located in China in a subcontractor already qualified and delivering in high volume for ST.

Former versus changed product:	The changed products will remain fully compliant with product datasheet in term of electrical, dimensional or thermal parameters. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in packing modes and standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Disposition of former products

Purpose is to implement additional production capacity, shipments will be done from all qualified assembly lines.

Marking and traceability

Marking is:

Assembly location	Plant and date code		
	Assy plant code	Assy year	Assy week
China (subco current line)	GP	**Y** (1 digit indicating the year)	**WW** (2 digits indicating the week number)
China (subco new line)	**GP**		

Traceability for the implemented change will be ensured by an **internal codification** and by the **Q.A. number**.

Qualification complete date	Week 14 - 2018

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Protection device	Transil™	SM6T6V8A	W15-2018
Protection device	Transil™	SM6T33CA	W18-2018
Protection device	Transil™	SM6T39CA	W15-2018

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
All	Week 15-2018	Week 28-2018

Comments:	With early PCN acceptance, possible shipments can be done on selected part numbers.

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	QRP18023 Attached

Reliability Evaluation Report

Qualification TVS protection devices in SMB package at Assembly/Test location in China

General Information		
Product Description	*Protection*	
Part Numbers		*SMBJ5.0A-TR*
		SMBJ5.0CA-TR
		SMBJ6.0A-TR
	SM6T6V8A	*SMBJ6.0CA-TR*
	SM6T6V8CA	*SMBJ6.5A-TR*
	SM6T7V5A	*SMBJ6.5CA-TR*
	SM6T7V5CA	*SMBJ8.5CA-TR*
	SM6T10A	*SMBJ10A-TR*
	SM6T10CA	*SMBJ10CA-TR*
	SM6T12A	*SMBJ12A-TR*
	SM6T12CA	*SMBJ12CA-TR*
	SM6T15A	*SMBJ13CA-TR*
	SM6T15CA	*SMBJ15A-TR*
	SM6T18A	*SMBJ15CA-TR*
	SM6T18CA	*SMBJ16A-TR*
	SM6T22A	*SMBJ18A-TR*
	SM6T22CA	*SMBJ18CA-TR*
	SM6T24A	*SMBJ20A-TR*
	SM6T24CA	*SMBJ20CA-TR*
	SM6T27A	*SMBJ22A-TR*
	SM6T27CA	*SMBJ22CA-TR*
	SM6T30A	*SMBJ24A-TR*
	SM6T30CA	*SMBJ24CA-TR*
	SM6T33A	*SMBJ26A-TR*
	SM6T33CA	*SMBJ26CA-TR*
	SM6T36A	*SMBJ28A-TR*
	SM6T36CA	*SMBJ28CA-TR*
	SM6T39A	*SMBJ30A-TR*
	SM6T39CA	*SMBJ30CA-TR*
		SMBJ33A-TR
		SMBJ33CA-TR
Product Group	*ADG*	
Product division	*ASD&IPAD*	
Package	*SMB*	
Maturity level step	*QUALIFIED*	

Locations	
Wafer fab	*ST TOURS FRANCE*
Assembly plant	*SUBCONTRACTOR SHANGHAI - CHINA*
Reliability Lab	*ST TOURS FRANCE*

Reliability Assessment
PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	28/03/2018	8	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
PCT / AC	Pressure Pot 2 bars / Autoclave
THB	Thermal Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test
IOLT / TF	Intermittent Operational Life Test / Thermal Fatigue
DPA	Destructive Physical Analysis
RSH	Resistance to Solder Heat
SD	Solderability

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

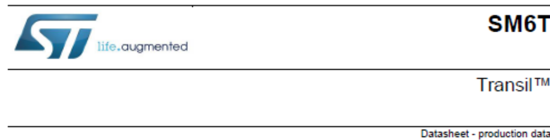
The aim of this report is to qualify according SMB package subcontractor in China for protection devices TVS 600W uni-directional and bi-directional with voltage below 39V (max VRM = 33V).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

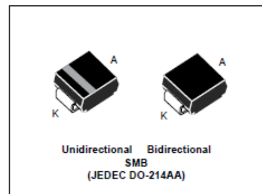
4.1 Device description



SM6T

Transil™

Datasheet - production data



Unidirectional Bidirectional
SMB
(JEDEC DO-214AA)

Features

- Peak pulse power:
  - 600 W (10/1000 µs)
  - 4 kW (8/20 µs)
- Stand-off voltage range: from 6.8 V to 220 V
- Unidirectional and bidirectional types
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating T_j max: 150 °C
- High power capability at T_j max.:
  - 515 W (10/1000 µs)
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-5
- MIL STD 883G, method 3015-7: class 3B:
  - 25 kV HBM (human body model)
- UL 497B, file number: QVGQ2.E136224
- Resin meets UL 94, V0
- MIL-STD-750, method 2026 solderability
- EIA STD RS-481 and IEC 60286-3 packing
- IPC 7531 footprint

Description

The SM6T Transil series are designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2 and MIL STD 883, method 3015, and electrical overstress according to IEC 61000-4-4 and 5. These devices are more generally used against surges below 600 W (10/1000 µs).

The Planar technology makes it suitable for high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

SM6T are packaged in SMB (SMB footprint in accordance with IPC 7531 standard).

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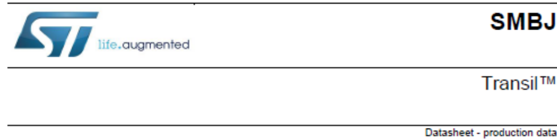
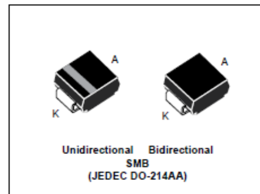


SMBJ

Transil™

Datasheet - production data



Unidirectional Bidirectional
SMB
(JEDEC DO-214AA)

Features

- Peak pulse power:
  - 600 W (10/1000 µs)
  - 4 kW (8/20 µs)
- Stand-off voltage range: from 5 V to 188 V
- Unidirectional and bidirectional types
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating T_j max: 150 °C
- High power capability at T_j max:
  - 515 W (10/1000 µs)
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-5
- MIL STD 883G, method 3015-7: class 3B:
  - 25 kV HBM (human body model)
- Resin meets UL 94, V0
- MIL-STD-750, method 2026 soldererability
- EIA STD RS-481 and IEC 60286-3 packing
- IPC 7531 footprint

Description

The SMBJ Transil series has been designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2, and MIL STD 883, method 3015, and electrical over stress according to IEC 61000-4-4 and 5. These devices are more generally used against surges below 600 W (10/1000 µs).

Planar technology makes these devices suitable for high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

SMBJ are packaged in SMB (SMB footprint in accordance with IPC 7531 standard).

Transil™ is a trademark of STMicroelectronics.

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4.2 Construction note

	SM6T / SMBJ
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS GLOBAL FRANCE
Technology / Process family	DISCRETE-TRANSIL / TAN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR SHANGHAI - CHINA
Package description	SMB CLIP (SOD 6 NEW)
Final testing information	
Testing location	SUBCONTRACTOR SHANGHAI - CHINA
Comments	

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Die Manufacturing plant	Assembly plant	Package	Comments
Lot 1	SM6T39CAY	ST TOURS	SUBCONTRACTOR CHINA	SMB	Qualification lot
Lot 2	SM6T6V8CAY				Qualification lot
Lot 3	SM6T36AY				Qualification lot

5.2 Test plan and results summary

Preconditioning MSL1 is done before some reliability tests (Y in PC column)

Test	PC	Std ref	Conditions	SS	Steps	Lot 1 SM6T39CAY	Lot 2 SM6T6V8CAY	Lot 3 SM6T36AY
HTRB	N	JESD22 A-108	Junction Temperature=150°C Tension=33.3V	80	168h	0/80	-	-
					504h	0/80	-	-
					1000h	0/80	-	-
HTRB	N	JESD22 A-108	Junction Temperature=150°C Tension=30.8V	78	168h	-	-	0/78
					504h	-	-	0/78
					1000h	-	-	0/78
HTRB	N	JESD22 A-108	Junction Temperature=150°C Tension=5.8V	80	168h	-	0/80	-
					504h	-	0/80	-
					1000h	-	0/80	-
TC	Y	JESD22 A-104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	317	500cy	0/80	0/80	0/77
					1000cy	0/80	0/80	0/77
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=30.8V	80	168h	-	-	0/80
					504h	-	-	0/80
					1000h	-	-	0/80
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=33.3V	80	168h	0/80	-	-
					504h	0/80	-	-
					1000h	0/80	-	-
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=5.8V	80	168h	-	0/80	-
					504h	-	0/80	-
					1000h	-	0/80	-
uHAST	Y	JESD22-A110-B	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	320	96h	0/80	0/80	0/80
MSL1 research	N	JESD22 A-113	Bake + 168h 85°C 85% + 3 IR reflows SAM before/after	30	168h	0/30	-	-
RSH	Y	ST 0060102 JESD22 A-111	Temperature=260°C Time (on)=10s	30	168h	0/30	-	-
DBT	N	DM 00112629	Fluxing followed by IR reflow. Visual inspection after DBT	30	Visual	Compliant	-	-
Solderability	N	JESD22 B-102	Steam Ageing SnAgCu bath	10	Visual	0/10	-	-
			Steam Ageing SnPb bath	10	Visual	0/10	-	-
			Dry Ageing SnAgCu bath	10	Visual	0/10	-	-
			Dry Ageing SnPb bath	10	Visual	0/10	-	-

Test	PC	Std ref	Conditions	SS	Steps	Lot 1 SM6T39CAY	Lot 2 SM6T6V8CAY	Lot 3 SM6T36AY
Repetitive Surge	Y	ADCS0060282	IPP=57A/µs Pulse delay=0.01ms	20	50 surges	-	0/20	-
			IPP=11.1A/µs Pulse delay=0.01ms	20	50 surges	0/20	-	-
			IPP=12A/µs Pulse delay=0.01ms	20	50 surges	-	-	0/20

6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Repetitive surges	ADCS0060282	Devices are submitted to rated Ipp for 1000 surges.	Purpose: This test is intended to verify robustness of device submitted to rated Ipp (as per data sheet) = exploration of reverse characteristic at a calibrated current value followed by the measure of voltage clamping value. Failure mode expected is short circuit of the device due to hot spot creation into silicon bulk at device periphery where the electrical field gradient is the most important. Physical analysis must be done to verify consistency of the failure mode and discriminate from extrinsic causes related to process escapes.
Package Oriented			
uHAST	JESD22 A-118	The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments .	Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
RSH Resistance to solder heat	ST 0060102 JESD22 B-106-A	Device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.

Test name	Standard Reference	Description	Purpose
PC Preconditioning	JESD22 A-113	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere..	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DBT Dead Bug Test	DM00112629	To evaluate the wettability of the SMD. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.