Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Transfer completion of Protection devices housed in SO8 package from ST Morocco to ST China
PCN Reference : ADG/16/10031

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

ITA6V5B1RL	ITA6V1U1RL	ESDA6V1U1RL
ITA18B1	ITA6V1U1	USB6B1
DA108S1	DA112S1	DA112S1RL
ESDA25B1	ESDA25B1RL	ITA6V5B1
USB6B1RL	ESDA6V1U1	DA108S1RL
ITA25B1	ITA18B1RL	ITA25B1RL
ITA10B1		

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STMicroelectronics
ADG - ASD & IPAD™ Division[1]
BU Protection

(1) ADG: Automotive and Discretes Group - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

PCN
Product/Process change notification

Transfer completion of Protection devices housed in SO8 package from ST Morocco to ST China

Notification number:	ADG-DIS/16/10031	**Issue Date**	12/12/2016
Issued by	Aline AUGIS		
Product series affected by the change		DA108S1 DA108S1RL DA112S1 DA112S1RL ESDA25B1 ESDA25B1RL ESDA6V1U1 ESDA6V1U1RL ITA10B1 ITA18B1 ITA18B1RL ITA25B1 ITA25B1RL ITA6V1U1 ITA6V1U1RL ITA6V5B1 ITA6V5B1RL ITA6V5C1RL USB6B1 USB6B1RL	
Type of change		Back end realization	

Description of the change

STMicroelectronics is finalizing its SO8 protection devices transfer from ST Morocco to ST China.

Reason for change

In order to improve the quality of the service, STMicroelectronics has decided to rationalize its production of Protection devices by transferring the assembly line to ST China plant.

ST China plant is already qualified and running protection devices in high volume on SO8 package line.

Former versus changed product:	The changed products will remain fully compliant with product datasheet in term of electrical, dimensional or thermal parameters. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either.

	The products remain in full compliance with the ST ECOPACK®2 grade ("halogen-free").

Disposition of former products

Deliveries of products released in Morocco back-end will continue as long as stocks are not completely depleted.

Marking and traceability

Parts produced in China are differentiated by their **marking** as indicated below

Assembly location	Assy plant code	Date code marking Assy year	Assy week
Morocco (ST)	CZ	**Y** (1 digit indicating the year)	**WW** (2 digits indicating the week number)
China (ST)	**GK**		

Traceability for the implemented change will be ensured by an **internal codification** and by the **Q.A. number**.

Qualification complete date	Week 37-2016

Forecasted sample availability

Product family	Commercial part Number	Availability date
Protection device	ITA25B1RL	Now
Protection device	USB6B1RL	Now

Other samples are available upon request.

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
All	Week 07-2017	Week 12-2017

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	16101QRP Attached

Reliability Evaluation Report

Qualification of Protection devices housed in SO8 package at ST Shenzhen plant

General Information	
Product Line	*Protection*
Product	*DA108S1 DA108S1RL DA112S1 DA112S1RL ESDA25B1 ESDA25B1RL ESDA6V1U1 ESDA6V1U1RL ITA10B1 ITA18B1RL ITA25B1 ITA25B1RL ITA6V1U1 ITA6V1U1RL ITA6V5B1 ITA6V5B1RL ITA6V5C1RL USB6B1 USB6B1RL*
Product Group	*ADG*
Product division	*ASD & IPAD*
Package	*SO 08*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST Tours (FRANCE)*
Assembly plant	*ST SHENZHEN (CHINA)*
Reliability Lab	*ST TOURS (FRANCE)*
Reliability assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1	16/09/2016	11	Aude DROMEL	Julien MICHELON	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditionning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
AC	Autoclave
u-HAST	Unbiast HAST
SD	Solderability
RSH	Resistance to Solder Heat
DBT	Dead Bug Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

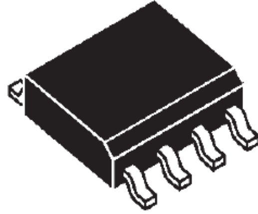
Objective is to transfer SO8 package for protection devices from ST Bouskoura assembly plant to ST Shenzhen plant.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

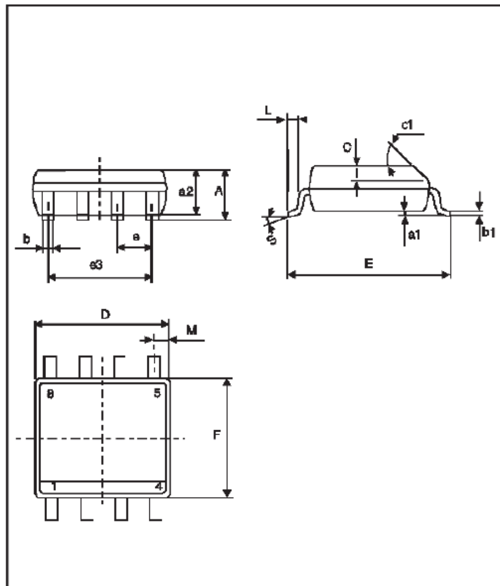


SO8

4.2 Device details : Package outline/Mechanical data

PACKAGE MECHANICAL DATA

SO8 (Plastic)



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C		0.50			0.020	
c1	45° (typ)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max)					

4.3 Construction note

	DA1xxS1/ESDAxx/USB6B1 / ITAxx
Wafer/Die fab. Information/	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	TRANSIL ASD
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS - FRANCE
Assembly information	
Assembly site	ST SHENZHEN - CHINA
Package description	SO-8
Final testing information	
Testing location	ST SHENZHEN - CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Die manufacturing plant	Assembly plant	Package	Comments
Lot 1	DALC112S1RLD	ST TOURS	ST SHENZHEN	SO 08	Qualification lots
Lot 2	ITA25B1RLD			SO 08	
Lot 3	USB6B1RLD			SO 08	

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		
						Lot 1	Lot 2	Lot 3
Die Oriented Tests								
HTRB	N	JESD22 A-108	Temperature=125°C Tension=24V	77	168h	-	0/77	-
					504h	-	0/77	-
					1000h	-	0/77	-
HTRB	N	JESD22 A-108	Temperature=150°C Tension=5.25V	77	168h	-	-	0/77
					504h	-	-	0/77
					1000h	-	-	0/77
HTRB	N	JESD22 A-108	Temperature=150°C Tension=15V	77	168h	0/77	-	-
					504h	0/77	-	-
					1000h	0/77	-	-
Package Oriented Tests								
MSL1	N	J-STD-020	Bake + 168h 85°C 85% + 3IR reflows + SAM before/after	90	168h	0/30	0/30	0/30
TC	Y	JESD22 A-104	-65°C/+150°C 2 cycles/h	75	500cy	0/25	0/25	0/25
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=5.25V	25	168h	-	-	0/25
					504h	-	-	0/25
					1000h	-	-	0/25
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=24V	25	168h	-	0/25	-
					504h	-	0/25	-
					1000h	-	0/25	-
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=15V	25	168h	0/25	-	-
					504h	0/25	-	-
					1000h	0/25	-	-
AC	Y	JESD22 A-102	Humidity (HR)=100% Temperature=121°C	50	96h	0/25	0/25	-
uHAST	Y	JESD22 A-110	Humidity (HR)=85% Temperature=130°C	25	96h	-	-	0/25
RSH	Y	JESD22 A-111	Dippings=2 Temperature=260°C	26	Visual	0/26	-	-
DBT	N	DM 00112629	Fluxing followed by IR reflow	30	Visual	0/30	-	-
SD	N	J-STD-002	Steam Ageing SnAgCu bath 245°C	10	Visual	0/10	-	-
			Steam Ageing	10	Visual	0/10	-	-

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		
						Lot 1	Lot 2	Lot 3
			SnPb 220°C					
			Dry Ageing SnAgCu 245°C	10	Visual	0/10	-	-
			Dry Ageing SnPb 220°C	10	Visual	0/10	-	-

6 TESTS DESCRIPTION

Test name	Standard Reference	Description	Purpose
		Die Oriented	
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
		Package Oriented	
HAST	JESD22-A110-B	The device is biased under 130°C 85% RH during 96 hours, or equivalent 110°C 85% RH during 264 hours, minimizing its internal power dissipation.	The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the "85/85" Steady-State Humidity Life Test (THB).
AC Autoclave	JESD22 A-102	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.

Test name	Standard Reference	Description	Purpose
RSH Resistance to solder heat	ST 0060102 JESD22 B-106-A	Device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere..	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.

Test name	Standard Reference	Description	Purpose
DBT	DM00112629	To evaluate the wettability of the SMD. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.