

PRODUCT/PROCESS CHANGE NOTIFICATION PCN13840 – Additional information

ASE KaoHsiung (Taiwan) LQFP 24x24 package copper palladium bonding wire introduction on STM32F2/F4/F7x and STM32H5/H7x listed products

MDG – General Purpose Microcontrollers Division (GPM)

What are the changes?

Changes described in table below:

	Existing ba	ick-end line	Added back-end line			
Assembly site			ASE KaoHsiung (Taiwan)			
Wire	Gold	0.8mil	CuPdAu 0.8mil			
GLUE	Sumitomo CRM 1076WA	YIZTECH 8143	Sumitomo CRM 1076WA	YIZTECH 8143	HITACHI EN4900G	
Marking composition	Withc	Without 2D		With 2D Marking		



How can the change be seen?



Codes already available on exisiting and added marking:

Y WW : Year Week (manufacturing date)



How to order samples?

- For all samples request linked to this PCN, please: place a <u>Non-standard</u> sample order (choose Sample Non Std Type from pull down menu) •
- insert the PCN number "PCN13840" into the NPO Electronic Sheet/Regional Sheet ٠
- request sample(s) through Notice tool, indicating a single Commercial Product for each request •

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Reliability Evaluation Report MDG-GPM-RER2303

ASEKH LQFP24x24 Low cost wire introduction

General Information	n	Traceability	
Commercial Product	STM32F427IIT6 STM32H725IGT6 STM32F745IET7 STM32F217ZGT6	Diffusion Plant	
Product Line	419X66 483X66 449x66 411X66	Assembly Plant	
Die revision	419 cut 2.2 483 cut 1.1 449 cut 1.1 411 cut 2.4		
Product Description	STM32F4xx STM32H7xx STM32F7xx STM32F2xx	Reliability Ass Pass Fail	essment X
Package	LQFP 176 24x24x1.4		
Silicon Technology	CMOSM40 CMOSM10		
Division	MDG-GPM		

Traceability	
Diffusion Plant	Crolles 300 TSMC Fab14 DIFF
Assembly Plant	SC ASE - TAIWAN

Reliability Assessment				
Pass	Х			
Fail				

Release	Date	Author	Function
1.0	02/06/2023	Gabin BOSCO	GPM BE Q&R

Approved by:

Name	Function	Location	Date
Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	ROUSSET	02/06/2023
Pascal NARCHE	Subgroup Quality Manager	ROUSSET	02/06/2023

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RELIABILITY EVALUATION OVERVIEW

• OBJECTIVE

The aim of this report is to present the reliability evaluation performed for the qualification of ASEKH (Taiwan) LQFP24x24 with copper-palladium wires on M10 and M40 technos.

PCN13840 changes are described here below:

	Existing ba	ck-end line	Added back-end line			
Assembly site						
Wire	Gold (D.8mil	CuPd 0.8mil			
GLUE	Sumitomo CRM 1076WA	YIZTECH 8143	Sumitomo CRM 1076WA	YIZTECH 8143	HITACHI EN4900G	
Marking compositi on	Without 2D		With 2D marking			

CONCLUSION

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

Package oriented tests have not put in evidence any criticality. Physical analysis performed on samples submitted to tests has not put in evidence any issue. ESD CDM are in accordance with ST spec.

Based on the overall results obtained, products below have positively passed reliability evaluation:

Line code	Commercial product	Diff plant	Assy plant
419X66	STM32F427IIT6	TSMC	
483X66	STM32H725IGT6		
449x66	STM32F745IET7	Crolles	ASEKH (TAIWAN)
411X66	STM32F217ZGT6		

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for all Finished Goods diffused in TSMC M10 and Crolles M10/M40, assembled in LQFP24x24 at ASEKH (Taiwan) in copper-palladium wires.

Refer to Section 3.0 for reliability test results.



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1. RELIABILITY STRATEGY

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 specification, in full compliancy with the JESD-47 international standard.

For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1. Generalities

Package line	Device (Partial RawLine Code)	Diffusion process	Number of lots
	1T*419	CMOSM10 TSMC	1
	1T*483	CMOSM40 Crolles	1
LQFF 24X24X1.4 176L	1T*449	CMOSM10 Crolles	1
	1T*411	CMOSM10 Crolles	1

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2.2. Traceability

2.2.1.Wafer Fab Information

Die 419 - LQFP24x24

Wafer Fab Information					
FAB1					
Wafer fab name / location	TSMC Taiwan / TSMC	Fab14 DIF	F		
Wafer diameter	12 inches				
Wafer thickness	775±25 μm				
Silicon process technology	CMOSM10				
Number of masks	44				
Die finishing front side (passivation) materials/Thickness	USG+NITRIDE/1,1µm				
Die finishing back side Materials	RAW SILICON				
Die area (Stepping die size)	25.43 mm ² (5582, 4556)				
Die pad size	Geometry Rectangular	Open(X,Y) 59,123 μm			
Sawing street width (X,Y)	80,80 µm				
	Wire bond pad metal	Composition		Thickness	
	1	TaN/Ta/CuSeed/Cu		0.22 µm	
	2	TaN/Ta/CuSeed/Cu		0.28 µm	
Metal levels/Materials/Thicknesses	3	TaN/Ta/C	CuSeed/Cu	0.28 µm	
	4 TaN/Ta/		CuSeed/Cu	0.28 µm	
	5 TaN/Ta/		CuSeed/Cu	0.28 µm	
	6	Ta/TaN/A	AlCu	0.73 µm	
	7	AlCu		1.2 µm	



Die 483 - LQFP24x24

Wafer Fab Information					
FAB1					
Wafer fab name / location	Crolles 300 / Crolles 300	12			
Wafer diameter	12 inches				
Wafer thickness	775±25 μm				
Silicon process technology	CMOSM40				
Number of masks	51				
Die finishing front side (passivation) materials/Thickness	PSG+NITRIDE/1,1µm				
Die finishing back side Materials	RAW SILICON				
Die area (Stepping die size)	15.66 mm ² (3753, 4175)				
Dia nod ciza	Geometry				
Die pad size	Die pad size Rectangular				
Sawing street width (X,Y)	80,80 µm				
	Wire bond pad metal	Composition	Thickness		
	1	Cu	0.11 µm		
	2	Cu	0.14 µm		
	3	Cu	0.14 µm		
Metal levels/Materials/Thicknesses	4	Cu	0.14 µm		
	5	Cu	0.14 µm		
	6	Cu	0.86 µm		
	7	Cu	0.86 µm		
	8	Ta/TaN/AlCu	1.525 µm		



Die 449 – LQFP24x24

Wafer Fab Information						
FAB1						
Wafer fab name / location	Crolles 300 / Crolles 300	12				
Wafer diameter (inches)	12					
Wafer thickness (µm)	775					
Silicon process technology	CMOSM10					
Number of masks	42					
Die finishing front side (passivation) materials	PSG NITRIDE					
Die finishing back side Materials	RAW SILICON					
Die area (Stepping die size)	26.913416 mm ² (5884, 4574)					
Dia nod oiza	Geometry	Open(X,Y)				
Die pad size	Rectangular	59,123 μm				
Sawing street width (X,Y) (µm)	80,80					
	Wire bond pad metal	Composition	Thickness			
	1	TaN/CuSeed/Cu	0.24 µm			
	2	TaN/CuSeed/Cu	0.33 µm			
Motal lovels/Materials/Thicknesses	3	TaN/CuSeed/Cu	0.33 µm			
Metal levels/materials/ I nicknesses	4	TaN/CuSeed/Cu	0.33 µm			
	5	TaN/CuSeed/Cu	0.33 µm			
	6	TaN/CuSeed/Cu	0.85 µm			
	7	AlCu/TinArc	1.45 µm			



Die 411 – LQFP 24x24

Wafer Fab Information						
FAB1						
Wafer fab name / location	Crolles 300 / Crolles 300	12				
Wafer diameter	12 inches					
Wafer thickness	775±25 μm					
Silicon process technology	CMOSM10					
Number of masks	42					
Die finishing front side (passivation) materials/Thickness	PSG+NITRIDE/1.1µm					
Die finishing back side Materials	RAW SILICON					
Die area (Stepping die size)	14.71 mm² (4006, 3674)					
	Geometry	Open(X,Y)				
Die pad size	Rectangular		59,123 µm			
	Rectangular		63,73 µm			
Sawing street width (X,Y)	80,80 µm		1			
	Wire bond pad metal	Compo	osition	Thickness		
	1	TaN/CuSeed/Cu		0.24 µm		
	2	TaN/Cu	uSeed/Cu	0.33 µm		
Metal levels/Materials/Thicknesses	3	TaN/CuSeed/Cu		0.33 µm		
	4 Ta		uSeed/Cu	0.33 µm		
	5	TaN/Cu	uSeed/Cu	0.33 µm		
	6	TaN/Cu	uSeed/Cu	0.85 µm		
	7	AlCu/T	inArc	1.45 µm		



2.2.2.Assembly Information

Package: LQFP 176 24x24x1.4	483	411 & 419				
Assembly plant name / location	ASE TAIWAN / SC ASE - TAIWAN					
Pitch	0.4mm					
Die thickness after back-grinding	375+/-25µm 300+/-25µm					
Die sawing method	l	_aser groove + mechanica	l sawing			
Bill of Material elements						
Lead frame/Substrate material/ reference	LF# A25472-0 LQ176L DR Pure tin C7025 SLOT PWB 6sq LF# A19506-0 FOR LQ 176L WITH SLOT 24					
Lead frame finishing (material/thickness)	Pure Tin (e3): Tolerance 7 to 20µm					
Die attach material/type(glue)/supplier	GLUE SUMITOMO EPOXY CRM HITACHI EN4900G GLUE YIZTECH 8 1076WA					
Wire bonding material/diameter	Copper-palladium 0.8 mils					
Molding compound material/supplier/reference	MOLDING RESIN SUMITOMO EME-G631SH MOLDING RESIN SUMITOMO EME-G631H					
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3					

2.2.3.Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, Rousset MDG Rel Lab, Shenzhen BE Lab

<u>Note:</u> ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: <u>http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html</u>



3. TEST RESULTS SUMMARY

3.1. Lot information

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
Lot 1	9R124619	419 cut 2.2	AA140007	201T*419CSX5		1 Reliability lot
Lot 2	VQ046607	483 cut 1.1	AA137095	201T*483CSXZ		1 Reliability lot
Lot 3	VQ205526	449 cut 1.1	AA228001	2A1T*449QCXZ	LQFF 170 24X24X1.4	1 Reliability lot
Lot 4	VQ111287	411 cut 2.4	AA140008	201T*411CSX2		1 Reliability lot

3.2. Test plan and results summary

ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h/30°C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	4	308	1 232	Lot 1: 0/308 Lot 2: 0/308 Lot 3: 0/308 Lot 4: 0/308	NA
HTSL	JESD22-A103	Ta= 150°C Duration= 1000hrs ☑ After PC	4	77	308	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77	NA
тс	JESD22-A104	Ta= -65/150°C Cyc= 500 ⊠After PC	4	77	308	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77	NA
THB	JESD22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 1000hrs ☑After PC	4	77	308	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77	NA
UHAST	JESD22-A118	Ta=130°C ,85% RH, 2 Atm Duration= 96hrs ☑ After PC	4	77	308	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77	NA



ELECTRICAL TEST VERIFICATION

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CDM	JEDEC JS-002	Voltage=500V for 411 Voltage=250V for	4	3	12	Lot 1: 0/3 Lot 2: 0/3 Lot 3: 0/3	NA
		449/419/483				Lot 4: 0/3	

PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
СА	Construction analysis including -Wire bond shear -Wire bond pull	ST internal specifications	4	50	200	Lot 1: 0/50 Lot 2: 0/50 Lot 3: 0/50 Lot 4: 0/50	NA

Note: Test method revision reference is the one active at the date of reliability trial execution.

4. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD 22-A103	High Temperature Storage Life
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104	Temperature cycling
JESD22-A110	Temperature Humidity Bake



5. GLOSSARY

ESD - CDM	Electrostatic Discharge - Charged device model
СА	Construction analysis
HTSL	Storage Life High temperature storage life
PC	Preconditioning
тс	Temperature Cycling
ТНВ	Temperature Humidity Bias
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
DMS	ST Advanced Documentation Controlled system/ Documentation Management system

6. REVISION HISTORY

Release	Date	Description
1.0	02/02/2023	Initial release



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