STMicroelectronics
IPD - ASD & IPAD Division[1]
BU Diodes & Rectifiers

(1) IPD: Industrial & Power Discretes - ASD: Application Specific Device - IPAD: Integrated Passive and Active Devices

PCN
Product/Process Change Notification

Die optimization for STPSCxxH065xx and STPSCxxTH13TI

Notification number:	9230	**Issue Date**	30-Apr-2015
Issued by	Aline AUGIS		

Product series affected by the change	STPSC10H065B-TR STPSC12H065D STPSC10H065D STPSC10H065DI STPSC10H065G-TR STPSC10TH13TI STPSC12H065CT STPSC16H065CT STPSC20H065CT STPSC20H065CW STPSC4H065B-TR STPSC4H065D STPSC4H065DI STPSC6H065B-TR STPSC6H065D STPSC6H065DI STPSC6H065G-TR STPSC6TH13TI STPSC8H065B-TR STPSC8H065CT STPSC8H065D STPSC8H065DI STPSC8H065G-TR STPSC8TH13TI
Type of change : new dice embedded improvements	Mask or mask set change with new die design

Description of the change

STMicroelectronics is now going to implement the new die optimization layout for its H series rectifier products in SiC 650V technology.

This change is related to a new SiC Junction Barrier Schottky (JBS) 650V die structure optimization. The electrical and thermal performances will be unchanged

Reason for change

This process qualification is the result of the constant investments made by STMicroelectronics in the SiC technology. It illustrates the commitment of the Company to reinforce its leading position in the SiC market.

This change enhances ST's competitiveness in SiC market by improving our positioning price/performances.

Former versus changed product:	▪ The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet ▪ The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. ▪ The footprint recommended by ST remains the same. ▪ There is no change in the packing modes and the standard delivery quantities either.

Disposition of former products

Former products will continue to be delivered as long as stock last

Marking and traceability

New internal codifications and QA numbers will be created to ensure full traceability.

Qualification complete date	April 2015 for STPSC6H065xx and STPSC10H065xx July 2015 for the remaining references

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Diodes & Rectifiers	Silicon Carbide Diodes	STPSC6H065D	May 2015
		STPSC10H065D	May 2015
		STPSC4H065D	July 2015
		STPSC8H065D	July 2015
		STPSC12H065D	July 2015
		STPSC10H065G-TR	July 2015
		Others	On request

Change implementation schedule

Perimeter	Estimated qualification	Estimated first shipments
STPSC6H065xx / STPSC10H065xx	April 2015	July 2015
STPSCxxH065xx / STPSCxxTH13TI	July 2015	Sept 2015

Customer's feedback Please contact your local ST sales representative or quality contact for requests concerning this change notification. Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change	
Qualification program and results	**15028QRP**

Reliability Evaluation Report

Qualification of STPSCxxH065xx and STPSCxxTH13TI (H series) with die optimization

General Information	
Product Line	*Rectifiers*
Product Description	*Silicon Carbide Power Schottky*
Product perimeter	*STPSCxxH065xx* *STPSCxxTH13TI*
Product Group	*IPG*
Product division	*ASD&IPAD*
Packages	*TO-220AC / TO-220AB* *TO-247* *TO-220AC Ins / TO-220AB Ins* *DPAK / D²PAK*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST CATANIA - ITALY*
Assembly plant	*ST SHENZHEN - CHINA*
Reliability Lab	*ST TOURS - FRANCE*
Reliability assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	30-Apr-2015	9	Isabelle BALLON	Julien MICHELON	Die optimization For SiC series H (STPSCxxH065xx and STPSCxxTH13TI)

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
HTRB	High Temperature Reverse Bias
HTFB	High Temperature Forward Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
IOLT	Intermittent Operating Life Test
PCT/AC	Pressure Cooker Test (Autoclave)
GD	Generic Data

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify die optimization layout for H series rectifier products in SiC 650V technology (STPSCxxH065xx and STPSCxxTH13TI), embedded in TO-220AC, TO-220AB, TO-247, TO-220AC Ins, TO-220AB Ins, DPAK, D²PAK packages.
The electrical and thermal performances of the products are unchanged.

The involved products are listed in the table below:

Product sub-Family	Product devices
Silicon Carbide Power Schottky Rectifiers	STPSCxxH065xx STPSCxxTH13TI

The reliability test methodology used follows the JESD47-H:« Stress Test Driven Qualification Methodology ».
The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- THB, PCT/AC to check the robustness to corrosion and the good package hermeticity.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Product	Packages
STPSCxxH065D	TO-220AC
STPSCxxH065CT	TO-220AB
STPSCxxH065CW	TO-247
STPSCxxH065B	DPAK
STPSCxxH065G	D²PAK
STPSCxxH065DI	TO-220AC Ins.
STPSCxxTH13TI	TO-220AB Ins.

4.2 Construction Note

	STPSCxx065xx & STPSCxxTH13TI
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA – ITALY
Technology / Process family	POWER SCHOTTKY SiC
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST CATANIA – ITALY
Assembly information	
Assembly site	ST SHENZHEN –CHINA
Package description	TO-220AC – TO-220AB – TO-247 – TO-220AC Ins – TO-220AB Ins DPAK – D²PAK
Molding compound	ECOPACK®2 (“Halogen-free”) molding compound for TO-220AC, TO-220AB, TO-220AC ins, TO-220AB Ins and TO-247 Epoxy molding compound for DPAK and D²PAK.
Lead finishing material	Lead free (pure Tin)
Final testing information	
Testing location	ST SHENZHEN -CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Commercial Product	Package	Comments
Lot 1	Generic part in SiC 6A 650V	TO-220AC	Similar optimized die layout
Lot 2	Generic part in SiC 12A 650V		Similar optimized die layout
GD1	STPSC25H12D		Similar periphery than optimized die layout
GD2	STPSC20H065CT	TO-220AB	Similar die design
GD3	STPSC20H065CW	TO-247	Similar die design
GD4	STPSC10TH13TI	TO-220AB Ins.	Similar die design
GD5	STPSC8H065G	D²PAK	Similar die design
GD6	STPSC15H12G		Similar periphery than optimized die layout
GD7	STPSC10H065B	DPAK	Similar die design

Detailed results in below chapter will refer to these references.

5.2 Test plan and results summary

Test	Std ref.	Conditions	SS	Steps / durat°	Failure/SS								
					L1	L2	GD1	GD2	GD3	GD4	GD5	GD6	GD7
Standard Tests													
HTRB	JESD22 A-108	VR = 0.8xVRRM Tj = 150°C Ta = Tj assumed	460	1000h		0/77	0/77	0/77	0/77	0/75		0/77	
		VR = VRRM Tj = 175°C Ta = Tj assumed	77	1000h	0/77								
HTFB	JESD22 A-108	Tj = 150°C	77	1000h	0/77								
THB	JESD22 A-101	85% RH, 85°C VR=100V	331	1000h	0/77	0/77	0/25		0/77		0/25	0/25	0/25
TC	JESD22 A-104	-65 / +150°C 2 cycles/hour	306	500cy		0/77	0/25	0/77	0/77	0/25	0/25		
			231	1000cy		0/77		0/77	0/77				
PCT (AC)	JESD22 A-102	121°C 2bar 100% RH	229	96h			0/25	0/77	0/77	0/25			0/25
IOLT	Mil Std 750 method 1037	ΔTc = 85°C t_{on} = t_{off} = 210s	231	8572cy	0/77		0/77	0/77					

6 ANNEXES

6.1 Tests description

Test name	Description	Purpose
	Die Oriented	
HTR(/F)B High Temperature Reverse(/Forward) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations; Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
	Package Oriented	
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
PCT (AC) Pressure Cooker Test (Autoclave)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.

7 COMPARATIVE ELECTRICAL PARAMETERS

STPSC6H065D Average values	Datasheet limit (Max.)	Reference (before die optimization)	With die optimization
IR 25°C 600V (µA)	60	5	4
IR 150°C 600V (µA)	250	50	33.5
VF 25°C at I0=6A (V)	1.75	1.56	1.5
VF 150°C at I0=6A (V)	2.5	1.98	1.8
IFSM 25°C at 10ms (A)	60	75	77
RTH(j-c) (°C/W)	2.4	1.6	1.6

STPSC10H065D Average values	Datasheet limit (Max.)	Reference (before die optimization)	With die optimization
IR 25°C 650V (µA)	100	8	4
IR 150°C 650V (µA)	425	85	50
VF 25°C at I0=10A (V)	1.75	1.56	1.5
VF 150°C at I0=10A (V)	2.5	1.98	1.8
IFSM 25°C at 10ms (A)	90	105	103
RTH(j-c) (°C/W)	1.5	1.25	1.1

Comparative measurements for datasheet parameters have revealed no impact in terms of electrical and thermal performances.