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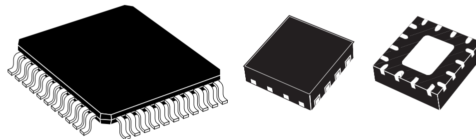
PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/15/9324

Analog, MEMS and Sensor Group (AMS)

Production transfer from Amkor Korea to Amkor Philippines for component packaged in QFP and QFN



QFP and QFN package

WHAT:

Progressing on the activities related to QFP and QFN manufacturing process, ST is ready to announce the transfer of these packages production capacity (assembly, test & finishing) for Analog MEMS and Sensors (AMS) group products from Amkor Korea to Amkor Philippines.
For reference, Amkor Philippines is already producing some other QFN type, SO and TSSOP packages for AMS group.

Material	Current process	Modified process
Assembly location	Amkor (Korea)	Amkor (Philippines)
Die attach	Sumitomo CRM 1085A (QFN4x4 and 9x9) ABLESTIK 8290 (QFN 8x8) Ablestik 3230 (QFP)	GLUE AMK-06 (QFN4x4) ABLESTIK 8290 (QFN 8x8) Ablestik 3230 (QFP)
Wire	Gold 1 mils / Gold 1.2Mils	Gold 1 mils / Gold 1.2Mils
Lead frame	Copper	Copper
Molding compound	SUMITOMO G700 (QFN) SUMITOMO G700L (QFP)	SUMITOMO G700 (QFN) SUMITOMO G700L (QFP)
Lead finishing	NiPdAgAu (QFN 4x4) Mate Tin (QFP, QFN 8x8 and 9x9)	NiPdAgAu (QFN 4x4) Mate Tin (QFP, QFN 8x8 and 9x9)
Test Location	ST Calamba Amkor Philippines St Muar (Malaysia) (QFN8x8) ST Grenoble (QFN9x9)	ST Calamba Amkor Philippines St Muar (Malaysia) (QFN8x8) ST Grenoble (QFN9x9)

Samples of test vehicles products are available and other products samples will be available upon request.

WHY:
To rationalize production capacity and improve service to ST Customers for the affected package.

HOW:
The change that covers AMS products packaged in QFN and QFP manufactured in Amkor Philippines is qualified through attached qualification plan. Here below you'll find the details.

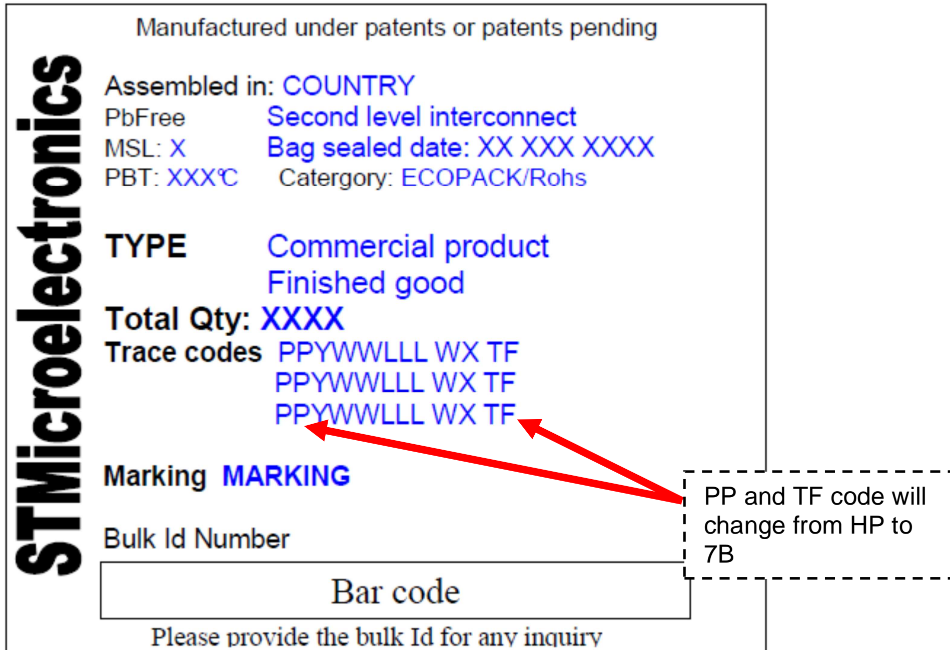
Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

WHEN:
The production for selected AMS products is forecasted in Q3 2015.
Production in Amkor Philippines for AMS Group is already running for more than 10 years for products in SO, TSSOP and some QFN.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled in Nantong Fujitsu will be ensured by marking on package and on label as per below description:



MSL: Moisture sensitivity level as per Jedec J–std-020C
PBT: Peak body temperature (maximum temperature for reflow soldering)
ECOPACK: present if leadfree component
TYPE: product name

Trace codes:
- PP: assembly plant code
- Y: last digit of the year of assembly
- WW: Week of assembly
- LL1: lot number
- WX: Diffusion plant code
- TF : Test&finishing plant code

Bulk ID number:
- 1: Product level (T for tested product)
- Y: last digit of the year
- P: Plant code
- WW: Week of labeling
- LOT: Sequential number for lot
- BOXX: Sequential number for box

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Qualification Report

General Information	
Product Line	*1203, L114, V519, F126, UJ17*
Product Description	NA
P/N	*TSA1203, TSL1014Y, STA529Q, SPIRIT1, STHV748QTR*
Product Group	*AMS*
Product division	AAS
Package	QFN, QFP
Silicon Process technology	HCMOS7A, BCD3, HCMOS8D, C090, BCD6S

Locations	
Wafer fab	*See table*
Assembly plant	*See table*
Reliability Lab	*Grenoble / Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	04-04-2015	29	Sandra Krief	JM Bugnard	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD22A-103	High Temperature Storage Life
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD22A-113	Preconditioning of Non hermetic Surface Mount Devices Prior to Reliability Testing
JESD22-A104	Temperature Cycling
JEP 150	Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled. Solid State Surface-Mount Components
SOP 2614	Reliability requirements for product qualification
0061692	Reliability tests and criteria for qualifications

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this qualification is to define and follow the qualification of Amkor Korea to Amkor Philippines transfer for AMS (Analog MEMS & Sensor Group).

3.2 Conclusion

This qualification is a package qualification, not a product qualification. Qualification Plan requirements have to be fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

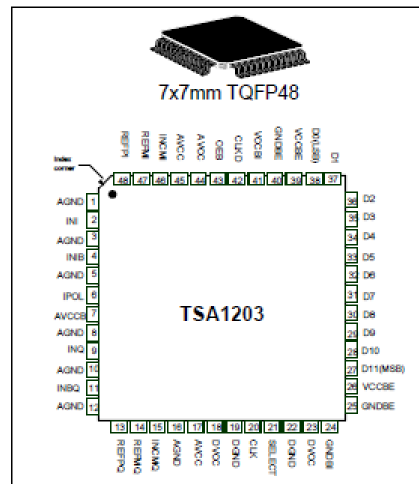
4.1 Device description

TSA1203

Dual-channel 12-bit 40Msps 215mW A/D converter

Features

- Low power consumption: 215 mW@40 Msps
- Single supply voltage: 2.5 V
- Independent supply for CMOS output stage with 2.5 V/3.3 V capability
- SFDR = -75 dBc @ F_{in} = 10 MHz
- 1GHz analog bandwidth track-and-hold
- Common clocking between channels
- Dual simultaneous sample and hold inputs
- Multiplexed binary word outputs
- Built-in reference voltage with external bias capability



Description

The TSA1203 is a new generation high-speed, dual-channel analog-to-digital converter implemented in a mainstream 0.25 µm CMOS technology that offers high performance and very low power consumption.

The TSA1203 is specifically designed for applications requiring a very low noise floor, high SFDR and good insulation between channels. It is based on a pipeline structure and digital error correction to provide high static linearity at F_S = 40 Msps, and F_{in} = 10 MHz.

Each channel has an integrated voltage reference to simplify the design and minimize external components. It is nevertheless possible to use the circuit with external references.

The ADC binary word outputs are multiplexed in a common bus with a small number of pins.
A tri-state capability is available for the outputs, allowing chip selection. The inputs of the ADC must be differentially driven.

The TSA1203 is available in extended temperature range (-40° C to +85° C), in a small 48-pin TQFP package.

Applications

- Medical imaging and ultrasound
- 3G base station
- I/Q signal processing applications
- High-speed data acquisition systems
- Portable instrumentation

December 2006 Rev 4 1/30

www.st.com

TSL1014

14 + 1 channel buffers for TFT-LCD panels

Datasheet – production data

Features

- Wide supply voltage: 5.5 V to 16.8 V
- Low operating current: 6 mA typical at 25 °C
- Gain bandwidth product: 1 MHz
- High current COM amplifier: ±100 mA output current
- Industrial temperature range: -40 °C to +85 °C
- Small package: TQFP48
- Automotive qualification

Application

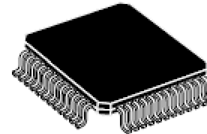
- TFT liquid crystal display (LCD)

Description

The TSL1014 device is composed of 14 + 1 channel buffers which are used to buffer the reference voltage for gamma correction in thin film transistor (TFT) liquid crystal displays (LCD).

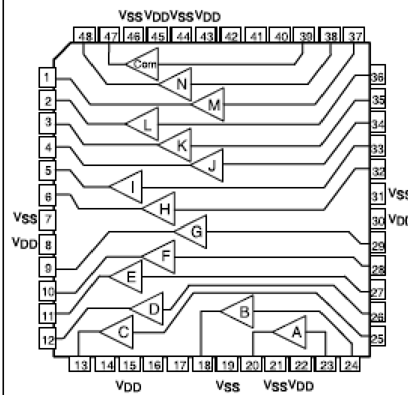
One “COM” amplifier is able to deliver high output current value, up to ±100 mA. Amplifiers A and B feature positive single supply inputs for common mode voltage behavior. The amplifiers C to N inclusive, and the COM amplifier, feature negative single supply inputs and are dedicated to the highest and lowest gamma voltages.

The TSL1014 device is fully characterized and guaranteed over a wide industrial temperature range (-40 to +85 °C).



7 x 7 mm TQFP48

Pin connections (top view)

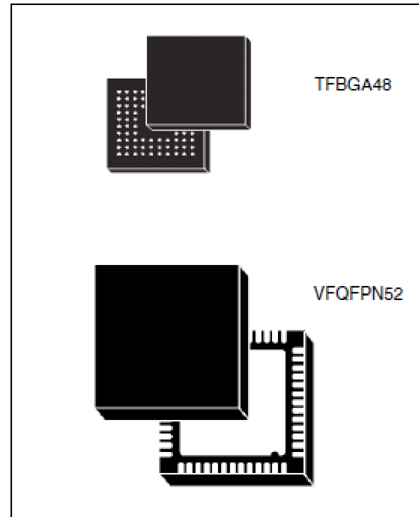


This is information on a product in full production.

STA529

FFX™ audio codec with analog and digital inputs and 2 x 1.2 W (or 2 x 100 mW HP) class-D amplifier

Datasheet – production data



Features

- Up to 96 dB dynamic range
- Sample rates from 8 kHz to 192 kHz
- FFX™ class-D driver
- 1.55 V to 1.95 V digital power supply
- 1.80 V to 3.60 V analog and I/O power supply
- 18-bit audio processing and class-D FFX™ modulator
- >90-dB SNR analog-to-digital converter
- Digital volume control:
  - +36 dB to -105 dB in 0.5-dB steps
  - Software volume update
- 16-bit ADC
- Individual channel and master gain/attenuation
- Automatic invalid input detect mute
- 2-channel I^2S input/output data interface
- Digitally controlled pop-free operation
- 90% efficiency
- Output power for stereo headphones or stereo speakers applications (at THD = 10% and V_{CC} = 3.3 V):
  - 45 mW with 32-Ω headphones
  - 85 mW with 16-Ω headphones
  - 720 mW with 8-Ω speakers
  - 1.1 W with 4-Ω speakers

Applications

- Portable devices
  - Laptops
  - Digital cameras
  - Microless applications

Table 1. Device summary

Order code	Operating temp. range	Package	Packaging
STA529Q	-40 to 85 °C	VFQFPN52	Tray
STA529	-40 to 85 °C	TFBGA48	Tray

This is information on a product in full production. www.st.com

SPIRIT1

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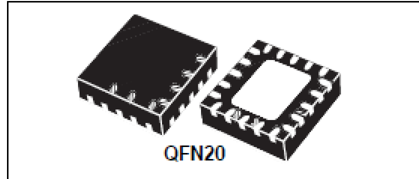
Low data rate, low power sub-1GHz transceiver

Datasheet - production data



Features

- Frequency bands: 150-174 MHz, 300-348 MHz, 387-470 MHz, 779-956 MHz
- Modulation schemes: 2-FSK, GFSK, MSK, GMSK, OOK, and ASK
- Air data rate from 1 to 500 kbps
- Very low power consumption (9 mA RX and 21 mA TX at +11 dBm)
- Programmable RX digital filter from 1 kHz to 800 kHz
- Programmable channel spacing (12.5 kHz min.)
- Excellent performance of receiver sensitivity (-118 dBm), selectivity, and blocking
- Programmable output power up to +16 dBm
- Fast startup and frequency synthesizer settling time (6 µs)
- Frequency offset compensation
- Integrated temperature sensor
- Battery indicator and low battery detector
- RX and TX FIFO buffer (96 bytes each)
- Configurability via SPI interface
- Automatic acknowledgment, retransmission, and timeout protocol engine
- AES 128-bit encryption co-processor
- Antenna diversity algorithm
- Fully integrated ultra low power RC oscillator
- Wake-up on internal timer and wake-up on external event
- Flexible packet length with dynamic payload length
- Sync word detection
- Address check
- Automatic CRC handling
- FEC with interleaving
- Digital RSSI output
- Programmable carrier sense (CS) indicator
- Automatic clear channel assessment (CCA) before transmitting (for listen-before-talk systems). Embedded CSMA/CA protocol
- Programmable preamble quality indicator (PQI)
- Link quality indication (LQI)
- Whitening and de-whitening of data
- Wireless M-BUS, EN 300 220, FCC CFR47 15 (15.205, 15.209, 15.231, 15.247, 15.249), and ARIB STD T-67, T93, T-108 compliant
- QFN20 4x4 mm RoHS package
- Operating temperature range from -40 °C to 105 °C

Applications

- AMR (automatic meter reading)
- Home and building automation
- WSN (wireless sensors network)
- Industrial monitoring and control
- Wireless fire and security alarm systems
- Point-to-point wireless link

Table 1. Device summary

Order code	Package	Packing
SPIRIT1QTR	QFN20	Tape and reel

This is information on a product in full production. www.st.com

4.2 Construction note

	120301 (TSA1203)	L11401 (TSL1014Y)	XX39 (other division product)	V51905 (STA529Q)	F126 (SPIRIT1/STS1TX)	UJ1701 (STHV748QTR)
Wafer/Die fab. information						
Wafer fab manufacturing location	ST Crolles (France)	ST Singapore	ST Agrate (Italy)	ST Rousset (France)	TSMC Taiwan	ST Agrate (Italy)
Technology	HCMOS7	BCD3S	BCD6S	HCMOS8D	90nm Generic TSMC	SOIBCD6S
Process family	HCMOS7	BCD	BCD	HCMOS8D-G	C90	SOIBCD
Die finishing back side	RAW SILICON	RAW SILICON	Cr/NiV/Au	RAW SILICON	RAW SILICON	Cr/NiV/Au
Die size mm	3.37 x 3.61	1.61 x 3.15	3.797 x 3.797	2.84 x 2.17	1.98 x 1.98	6.106 x 5.933
Bond pad metallization layers	AlCu	Ti/TiN/AlSiCu	AlCu + Thick Cu with Alu-cap	Ti/Al/TiN	TaN/Ta/Cu/Cu/Al Cu	Ti/AlCu/TiN
Passivation type	P-VAPOX(SiO2) / NITRIDE (SiN)	USG-PSG-SiON-PIX	SiN/TEOS/SiN	P-VAPOX(SiO2) / NITRIDE (SiN)	PSG + NITRIDE	TEOS/SiN/ Polyimide
Wafer Testing (EWS) information						
Electrical testing manufacturing location	ST GRENOBLE	ST SINGAPORE		ST Agrate	ST SINGAPORE	ST GRENOBLE
Assembly information						
Assembly site	ATP1	ATP1	ATP1	ATP1	ATP3	ATP1
Package description	LQFP7x7 48leads	LQFP7x7 48leads	TQFP7x7ePad 32leads	VFQFPN8x8 52leads	VFQFPN4x4 20leads	VFQFPN9x9 64leads
Molding compound	G700L	G700L	G700L	G700	G700	G700
Frame material	Cu	Cu	Cu	Cu	Cu	Cu
Die attach process	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue
Die attach material	Ablestick 3230	Ablestick 3230	Ablestick 3230	Ablestick 8290	Sumitomo CRM 1085A	Sumitomo CRM 1085A
Die pad size µm	75x90	76x76		65x70	53x66	81x81
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Au 1 mils	Au 1 mils	Au, 1.3 mils	Au 1 mils	Au 1 mils	Au 1.2 mils
Lead finishing/bump solder material	Sn	Sn	Sn	Sn	NiPdAgAu	Sn
Final testing information						
Testing location	ST Grenoble	ST Philippines		ST MUAR	ATP3	ST CATANIA

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Trace Code	Package	Raw Line	Comments
1	7B439534	QFP48	HB5B*1203AAA	
2	7B440324	QFP48	HB5B*L114AC6	
3	ER000312AG6053	QFP32	BA3Q*UM39AAV	Other division test vehicle
4	7B440522	QFN 52	HB90*V519ACG	
5	7B442A4T	QFN 20	HBZU*F126AD9	
6	7B443393	QFN 64	EBLT*UJ17AAA	

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS						
						1203	L114	XX39	V519	SPIRIT1	UJ17	Comment
Die Oriented Tests												
HTB	N	JESD22 A-108	Tj = 125°C, BIAS	80	168 H	0/78	0/78			0/78		
					500 H	0/78	0/78			0/78		
					1000 H	0/78	0/78			0/78		
HTSL	N	JESD22-A103	T=150°C / 1000H	80	500 H			3x0/60			45	
					1000 H			3x0/60			45	
ELFR	N	AEC Q100 - 008	Tamb=125°C with Tj<160°C	800	48 H		800					
Package Oriented Tests												
PC		JESD22 A-113	Drying 24 H @ 125°C Store 192h @ 30°C / 60% RH Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/78	0/78	3x0/77*	0/78		77	* 100 thermal cycling -50/+150°C before AC
TC	Y	JESD22 A-104	Ta = -50°C to 150°C		100 cy	0/78	0/78	3x0/77	0/78	0/78	77	
					200 cy		0/78	3x0/77	0/78	0/78	77	
					1000 cy	0/78	0/78	3x0/77	0/78	0/78	77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H		0/78			0/52	77	
					500 H		78			0/52	77	
					1000 H		78			0/52		
Other Tests												
ESD	N	AEC Q101-001, 002 and 005	CDM	3	kV	1.5 kV PASS	3			1kV PASS		
SD	N		After ageing 8h and 16h	50			PASS		PASS	PASS		
BPS	N	MIL – STD683	Bond Pull Strength	50	30 bonds / 5 devices		5		PASS			
PD	N	AECQ100 - 001	Physical dimension	5			PASS		PASS	PASS		

4 Annexes

4.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
Package Oriented		
AC **autoclave**	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC **Temperature Cycling**	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB **Temperature Humidity Bias**	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

5 GLOSSARY

ESD Electro Static Discharge
ELFR Early Life Failure Rate
GL Gate Leakage
HTB High Temperature Bias
HTRB High Temperature Reverse Bias
HTS High Temperature Storage
T.H.B. Temperature Humidity Bias
T.C. Thermal Cycle
P.P. Pressure Pot
P.C. Preconditioning