



Reliability Evaluation Report

On

M02 VIPOWER Transfer from CT6 to AMK6

TV: VN330SP-E

General Information		Locations	
Product Line	VN3301	Wafer fab	Singapore 6
Product Description	Quad high-side smart power solid state-relay		
P/N	VN330SP-E	Assembly plant	MUAR B/E
Product Group	AMG		
Product division	IND. & POWER CONV.	Reliability Lab	AMG Catania Reliability Lab
Package	PowerSO-10	Reliability assessment	Pass
Silicon Process technology	VIP - M02		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Oct-2016	6	Vito Gisabella Alfio Riciputo	Giovanni Presti	

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

The VN330SP-E is a monolithic device made using STMicroelectronics VIPower technology, intended for driving four independent resistive or inductive loads, with one side connected to ground.

3.1 Objectives

M02 VIPOWER transfer from CT6 to Singapore 6.

The Reliability verification will be performed by TVs.

The present report is related to the 1st Lot of TV VN33 line.

3.1.1 Evaluation Plan

The evaluation plan will includes the following TVs:

Test Vehicle (line)	Diffusion Lot	Assy Lot	Package	FE Tech	Comment
VN33	Singapore Ang Mo Kio	MUAR B/E	PowerSO-10	VIP M02	1 st Lot
VN34	Singapore Ang Mo Kio	MUAR B/E		VIP M02	2 nd Lot
VN33	Singapore Ang Mo Kio	MUAR B/E		VIP M02	3 rd Lot



3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The VN330SP-E is a monolithic device made using STMicroelectronics VIPower technology, intended for driving four independent resistive or inductive loads, with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shut-down protects the chip from overtemperature and short circuit. The open drain diagnostic output indicates overtemperature conditions.

4.2 Construction note

	VN330SP-E
Wafer/Die fab. information	
Wafer fab manufacturing location	Singapore 6 Ang Mo Kio
Technology	VIP M02
Die finishing back side	Ti/NiV/Au
Die size	5400 x 4500 micron
Passivation type	SiN (nitride)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	QT200
Assembly information	
Assembly site	MUAR
Package description	PowerSO-10
Molding compound	Epoxy
Frame material	FRAME PSO-10 4riv Flo SpAg
Die attach material	PREFORM
Wires bonding materials/diameters	WIRE Au D1.3
Final testing information	
Testing location	MUAR B/E
Tester	QT200



5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot	Technical Code	Package	Comments
LOT # 1	AMIY*VN33DY6	PowerSO-10	

5.2 Test plan and results summary

VN330SP-E

Test	PC	Std ref.	Conditions (*)	SS	Steps	Failure/SS	Note
Die Oriented Tests							
HTS	N	JESD22 A-103	Ta = 150°C		168 H	0/45	
					500 H	0/45	
					1000 H	0/45	
HTOL	N	JESD22 A-108	Ta = 125°C Vcc1=+28V Vcc2=+5V		168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 40 H @ Ta=60°C Rh=60% Oven Reflow @ Tpeak=250°C 3 times		Final	Pass	Go no go
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96H	0/25	Eng. evaluation
					168 H	0/25	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	
					200 cy	0/25	
					500 cy	0/25	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85% Vcc1=+24V		168 H	0/25	
					500 H	0/25	
					1000 H	0/25	
(*) all samples have been assembled on dedicated PCB							
Other Tests							
ESD	N	ANSI/ESDA/JED EC JS001-2014	HBM	3	+/- 2000V	0/3	
		ANSI/ESDA/JED EC JS002-2014	CDM	3	+/-500V All pins	0/3	
			CDM	3	+/-750V Corner Pins	0/3	
		EIA/JESD78E	LU	6	+/-100mA	0/6	



6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model HBM: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed	To verify the presence of bulk parasitic effect inducing latch-up.



Reliability Evaluation Report

On
M02 VIPOWER Transfer from CT6 to AMK6
TV: VN340SP-E

General Information	
Product Line	VN3401
Product Description	Quad high-side smart power solid state-relay
P/N	VN340SP-E
Product Group	AMG
Product division	IND. & POWER CONV.
Package	PowerSO-10
Silicon Process technology	VIP-M02

Locations	
Wafer fab	Singapore Ang Mo Kio
Assembly plant	MUAR
Reliability Lab	Catania Reliability Lab
Reliability assessment	Pass

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

The VN340SP-E is a monolithic device developed using ST VIPower™ technology, intended to drive four independent resistive or inductive loads with one side connected to ground.

3.1 Objectives

Transfer M02 VIPOWER from CT6 to Singapore Ang Mo Kio.

The Reliability verification will be performed by TVs.

The present report is related to the 2nd Lot of TV VN34 line.

3.2 Evaluation Plan

The evaluation plan will include the following TVs:

Test Vehicle (line)	Diffusion Lot	Assy Lot	Package	FE Tech	Comment
VN33	Singapore Ang Mo Kio	MUAR B/E	PowerSO-10	VIP M02	1 st Lot
VN34	Singapore Ang Mo Kio	MUAR B/E		VIP M02	2 nd Lot
VN33	Singapore Ang Mo Kio	MUAR B/E		VIP M02	3 rd Lot

3.3 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



4 DEVICE CHARACTERISTICS

4.1 Device description

The VN340SP-E is a monolithic device developed using ST VIPower™ technology, intended to drive four independent resistive or inductive loads with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. The open drain diagnostic output indicates overtemperature conditions. Each I/O is pulled down when the overtemperature condition of the relative channel is verified.

4.2 Construction note

	VN340SP-E
Wafer/Die fab. information	
Wafer fab manufacturing location	SINGAPORE Ang Mo Kio
Technology	VIP M02
Die finishing back side	Ti/NiV/Au
Die size	5070 x 4390 micron
Passivation type	SiN (nitride)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	QT200
Assembly information	
Assembly site	MUAR B/E
Package description	PowerSO-10
Molding compound	Epoxy
Frame material	FRAME PSO-10 4riv Flo SpAg
Die attach material	PREFORM
Wires bonding materials/diameters	WIRE Au D1.3
Final testing information	
Testing location	MUAR B/E
Tester	QT200



5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot	Technical Code	Package	Comments
Lot #1	AMIY*VN34EY6	PowerSO-10	

5.2 Test plan and results summary

VN340SP-E

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
Die Oriented Tests							
HTS	N	JESD22 A-103	Ta = 150°C		168 H	0/45	
					500 H	0/45	
					1000 H	0/45	
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					1000 H	0/77	
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					168 H	0/25	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	
					200 cy	0/25	
					500 cy	0/25	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85% Vcc1=+24V		168 H	0/25	
					500 H	0/25	
					1000 H	0/25	

(*) all samples have been assembled on dedicated PCB

Other Tests							
ESD	N	ANSI/ESDA/JEDEC C JS001-2014	HBM	3	+/- 2000V	0/3	
		ANSI/ESDA/JEDEC C JS002-2014	CDM	3	+/-500V All pins	0/3	
			CDM	3	+/-750V Corner Pins	0/3	
		EIA/JESD78E	LU	6	+/-100mA	0/6	



5.3 Tests Description

Test name	Description	Purpose
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Public Products List

Public Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Additional wafer fab in ST Ang Mo Kio (Singapore) for VIPOWER M02 products

PCN Reference : AMG/17/10123

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

VN340SP-33-E	VN340SP-E	VN540SP-E
VN540SPTR-E	VN330SP-E	VN340SPTR-33-E
VN540-E	VN340SPTR-E	VN330SPTR-E



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