Reliability Report

New Product Qualification

HBIP40 Technology Introduction for the 5V and 3.3V Output Voltage versions of the L78L Product Family

Test Vehicles:

L78L05CD13TR
L78L05CD13TR
L78L33ABUTR

General Information	
Product Line	LA0501 LA0501 LA3301
Product Description	5V 100mA Pos. Reg 5V 100mA Pos. Reg. Adjustable voltage regulator
P/N	L78L05CD13TR L78L05CD13TR L78L33ABUTR
Product Group	AMG (Analog & MEMS Group)
Product division	General Purpose Analog & RF Division Power Management
Package	SO 08, Cu wire SOT 89, Au wire
Silicon Process technology	Bip HF - HBIP40V

Locations	
Wafer fab	Singapore Ang Mo Kio
Assembly plant	SO 08 Shenzhen B/E SOT 89 NANTONG FUJITSU
Reliability Lab	ADG Catania Reliability Lab
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	March 2016	7	Alfio Rao	Giovanni Presti	Final report

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Linear Voltage Regulators: HBIP40 Technology Introduction for the 5V and 3.3V Output Voltage versions of the L78L Product Family

Test Vehicles:

- L78L05CD13TR SO 08 Cu Wire 1st diff. Lot
- L78L05CD13TR SO 08 Cu Wire 2nd diff. Lot
- L78L33ABUTR SOT 89 Au Wire 3rd diff. Lot

HBIP40 is a technology already qualified by STM

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

SO-8

SOT-89

The L78L series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat-sink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or oncard regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The L78L series used as Zener diode/resistor combination replacement, offers e improvement along with lower quiescent current and lower noise.

4.2 Construction note

	L78L05CD13TR (1st Lot - HBIP40)	L78L05CD13TR (2nd Lot - HBIP40)	L78L33ABUTR (3nd Lot - HBIP40)
Wafer/Die fab. information			
Wafer fab manufacturing location	Singapore Ang Mo Kio		
Technology	Bip HF		
Process family	HBIP40V		
Die finishing back side	LAPPED SILICON		
Die size	766 x 706 micron		
Passivation type	P-VAPOX/NITRIDE		
Wafer Testing (EWS) information			
Electrical testing manufacturing location	Ang Mo Kio EWS		
Tester	ETS 300		
Tester Program	LA05QAE01	LA05QAE01	LA33QAE01
Assembly information			
Assembly site	Shenzhen B/E	Shenzhen B/E	NANTONG FUJITSU
Package description	SO 08	SO 08	SOT 89
Molding compound	Epoxy	Epoxy	Epoxy
Frame material	SO 8L 94x125 SHD OpB 4+2+2 4Layers	SO 8L 94x125 SHD OpB 4+2+2 4Layers	SOT89-3A/75*70mil
Die attach material	GLUE	GLUE	GLUE
Wires bonding materials/diameters	1.0 mils - Cu	1.0 mils - Cu	1,0 mils-Au
Final testing information			
Testing location	ST Shenzhen	ST Shenzhen B/E	NANTONG FUJITSU
Tester	ASL1000 / qt200	ASL1000	ASL1000
Test Program	L78L05C.prg / LAXXFC05.CTS	L78L05C.prg	L78L33ABD_LA33_02

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Technical Code	Package	Product Line	Comments
1	ZPO7*LA05BA6	SO 08	LA0501	HBIP40V
2	ZPO7*LA05BA6	SO 08	LA0501	HBIP40V
3	1F39*LA33BA6	SOT 89	LA3301	HBIP40V

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1 SO8	Lot 2 SO8	Lot 3 Sot89	
Die Oriented Tests									
HTOL	N	JESD22 A-108	Ta = 125°C Vcc= +30V		168 h	0/77	0/77		
					500 h	0/77	0/77		
					1000 h	0/77	0/77		
HTSL	N	JESD22 A-103	Ta = 150°C		168 h	0/45	0/45	0/45	
					500 h	0/45	0/45	0/45	
					1000 h	0/45	0/45	0/45	
HTSL	N	JESD22 A-103	Ta = 175°C		168 h	0/45	0/45		Engineering evaluation on Cu wire
					500 h	0/45	0/45		
					1000 h	0/45	0/45		
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	Pass		Pass	
AC	Y	JESD22 A-102	Pa= 2Atm / Ta=121°C		168 h	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, Vcc1= +24V		168 h	0/77	0/77		
					500 h	0/77	0/77		
					1000 h	0/77	0/77		
Other Tests									
ESD	N	ANSI/ESDA/JEDEC JS001	HBM +/- 2000V	3	2KV	Pass			
		ANSI/ESD S5.3.1	CDM 500V	3	500V	Pass			

6 TESTS DESCRIPTION

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Test		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model HBM: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.