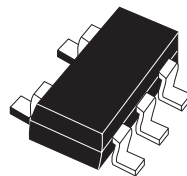


**PRODUCT/PROCESS
CHANGE NOTIFICATION**

PCN AMG/16/9781

Analog and MEMS Group (AMG)

**Additional production capacity in Fujitsu (Nantong/China) for selected CP in SOT23-5 package
(General Purpose Analog/AMG)**



Sot23-5

WHAT:

Progressing on the activities related to Sot23-5 manufacturing processes expansion, ST is glad to announce an additional production capacity in ST's subcontractor Fujitsu (Nantong/China) for selected CP of General Purpose Analog (GPA).

Logic products from AMG are already produced in Nantong Fujitsu since 2011 and other analog products since 2012.

Production will be done both in Carsem and Fujitsu (second source).

Material	Current process	Modified process
Assembly location	Carsem (Malaysia)	Fujitsu (Nantong/China)
Die attach	QMI519	Ablestik 8200T
Wire	Gold 1Mil	Gold 1Mil
Leadframe	Copper	Copper
Molding compound	Hitachi CEL8240HF10LXC	Sumitomo EMEG600
Leadfinishing	NiPdAu	Sn

For the complete list of the part numbers affected by the change, please refer to the attached Products list.

WHY:

To improve service to ST Customers and increase capacity for the affected product.

HOW:

The change that covers additional General Purpose Analog (GPA) products is already qualified through the attached report.

Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

WHEN:

Production in Fujitsu (Nantong/China) for selected GPA product is forecasted end of June 2016.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by marking on label as per below description:

STMicroelectronics	Manufactured under patents or patents pending	
	Assembled in:	COUNTRY
	PbFree	Second level interconnect
	MSL: X	Bag sealed date: XX XXX XXXX
	PBT: XXX°C	Catergory: ECOPACK/Rohs
	TYPE	Commercial product Finished good
	Total Qty:	XXXX
	Trace codes	PPYWWLLL WX TF PPYWWLLL WX TF PPYWWLLL WX TF
	Marking	MARKING
	Bulk Id Number	
Bar code		
Please provide the bulk Id for any inquiry		

PP and TF code will change from 9Y to GF

MSL: Moisture sensitivity level as per Jedec J-std-020C

PBT: Peak body temperature (maximum temperature for reflow soldering)

ECOPACK: present if leadfree component

TYPE: product name

Trace codes: PP: assembly plant code

Y: last digit of the year of assembly

WW: Week of assembly

LL1: lot number

WX: Diffusion plant code

TF : Test&finishing plant code

Bulk ID number: 1: Product level (T for tested product)

Y: last digit of the year

P: Plant code

WW: Week of labeling

LOT: Sequential number for lot

BOXX: Sequential number for box

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.

There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.

Reliability Report

*Halogen free material set in Nantong Fujitsu
(China) for Hirel & Standard products in Sot23-5*

General Information		Locations	
Product Line	VG08, 0391 RR3301	Wafer fab	ST Singapore
Product Description	SINGLE 2-INPUT AND GATE, Single comparator, Ultra Low Drop Vreg@50mA 3.3 V 74V1G08STR	Assembly plant	Nantong Fujitsu (China)
P/N	TS391ILT, LD2980CM33TR	Reliability Lab	IMS-APM Catania Reliability Lab
Product Group	AMS (Analog, Mem's and Sensor) APM (Analog Power and Mems)		
Product division	Analog division IPC		
Package	SOT 23-5L HCMOS4T		
Silicon Process technology	Bipolar BI20II		

DOCUMENT INFORMATION

Version	Date	Pages	Approved by	Comment
1.0	30/11/2011	8	JM Bugnard	First issue
2.0	10/09/2012	8	JM Bugnard	To add bipolar test vehicle
3.0	11/04/2016	9	JM Bugnard	To add electrical comparison TS321

Reference document

Version	Date	Ref	Approved by	Comment
1.1	23-Nov-2011	REL-6043-282.11/MSN-095	Giovanni Presti	Final report
1.1	09-Nov-2010	REL-6043-369.10/GCP.097	Giovanni Presti	Final Report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
 This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.



TABLE OF CONTENTS

- 1 APPLICABLE AND REFERENCE DOCUMENTS6**
- 2 GLOSSARY6**
- 3 RELIABILITY EVALUATION OVERVIEW6**
 - 3.1 OBJECTIVES6
 - 3.2 CONCLUSION6
- 4 DEVICE CHARACTERISTICS7**
 - 4.1 DEVICE DESCRIPTION7
 - 4.2 CONSTRUCTION NOTE7
- 5 TESTS RESULTS SUMMARY8**
 - 5.1 TEST VEHICLE8
 - 5.2 TEST PLAN AND RESULTS SUMMARY8
 - 5.3 TESTS DESCRIPTION10
- 6 ANNEXES:11**
 - 6.1 DEVICE DETAILS11
 - 6.2 PACKAGE OUTLINES12
 - 6.3 MECHANICAL DATA13

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify halogen free material set for Sot23-5 package assembled in Nantong Fujitsu for Hirel & Standard products.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

74V1G08STR: The 74V1G08 is an advanced high-speed CMOS SINGLE 2-INPUT AND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C2MOS technology. The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output. Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

LD2980CM33TR: The low drop-voltage and the ultra low quiescent current make them suitable for low noise, low power applications and in battery powered systems. The quiescent current in sleep mode is less than 1 μ A when the INHIBIT pin is pulled low. A shutdown logic control function is available on pin n° 3 (TTL compatible). This means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption.

The LD2980 is designed to work with low ESR ceramic capacitors. Typical applications are cellular phone, laptop computer, personal digital assistant (PDA), personal stereo, camcorder and camera.

TS391ILT: This device consists of a low-power voltage comparator designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

This comparator also has a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

4.2 Construction note

	74V1G08STR	TS391ILT	LD2980CM33TR
Wafer/Die fab. information			
Wafer fab manufacturing location	ST Singapore		
Technology	HCMOS4T	Bipolar	BI20II
Process family	MOS	BIP111	CD BI20II
Die finishing back side	LAPPED SILICON		
Die size	652 X 402 μ m	1070x770	1470, 990 μ m
Bond pad metallization layers	AlSiCu	AlSiCu	AlSi
Passivation type	PSG + NITRIDE	nitride	P-VAPOX/NITRIDE/POLYIMIDE
Wafer Testing (EWS) information			
Electrical testing location	ST Singapore		
Tester	QT 200	ASL 1K	N/A
Assembly information			
Assembly site	NFME		
Package description	Sot23-5		
Molding compound	EMEG600 Sumitomo		
Frame material	Copper		
Die attach process	Epoxy dispensing		
Die attach material	8200T ABLESTIK		
Die pad size	1.68*1.21mm		
Wire bonding process	Thermosonic Ball bonding		
Wires bonding materials/diameters	1.0mils Au wire		
Lead finishing process	plating		
	100% Sn		
Final testing information			
Testing location	NFME		
Tester	ASL1K	ASL 1K	STS8200



5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Source lot	Assy Lot	Process/ Package	Product Line	Comments
1	60439V5B	1TF31040101	HCMOS4/ Sot23-5	VG0801	
2	6148XJF	6F205031	Bipolar/Sot23-5	0391	
3	6010JKH	0TF20870101	BI20II / Sot23-5	RR33	Other ST divisions results
4	6010JKH	0TF22060101	BI20II / Sot23-5	RR33	Other ST divisions results

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 1	Lot 2	Lot3	Lot 3	
Die Oriented Tests										
HTB	N	JESD22 A-108	Tj = 125°C, BIAS	154	168 H	0/77	2x0/78			
					500 H	0/77	2x0/78			
					1000 H	0/77	2x0/78			
HTSL	N	JESD22 A-103	Ta = 150°C	135	168 H	0/45	0/78		0/45	
					500 H	0/45	0/78		0/45	
					1000 H	0/45	0/78		0/45	
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	693	Final	PASS	PASS	Pass	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	231	96 H	0/77		0/77	0/77	
					168 H	0/77		0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	231	100 cy	0/77		0/77	0/77	
					200 cy	0/77		0/77	0/77	
					500 cy	0/77		0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS	231	168 H	0/77	0/78	0/77	0/77	
					500 H	0/77	0/78	0/77	0/77	
					1000 H	0/77	0/78	0/77	0/77	
ESD	N	AEC Q101-001, 002 and 005	CDM	3	1kV	PASS				



Electrical comparison TS321

Limits	OQA 1FT 2WS	UTL	LTL	Mode	Fujitsu					Carsem				
					Min	Average	Max	Stdev	CPK	Min	Average	Max	Stdev	CPK
P101_A0	Vio	10	-10	mV	-2.76	0.63	3.37	0.46	6.78	-2.41	0.79	3.47	0.62	4.94
P117_A1	Voh	none	27	V	28.74	28.76	28.79	0.01	73.79	28.50	28.51	28.53	0.01	87.58
P102_A1	lio	30	-30	nA	-15.05	-10.99	-2.90	0.89	N/A	-3.97	1.41	7.84	1.36	N/A
P103_A1	libn	0	-150	nA	-38.33	-33.14	-23.83	2.05	N/A	-31.89	-25.74	-15.53	2.61	N/A
P103_A1	libp	0	-150	nA	-25.09	-22.15	-17.12	1.56	N/A	-32.01	-27.15	-19.56	2.02	N/A
P106_*1	lcc	0.8	0.18	mA	0.55	0.57	0.58	0.00	17.95	0.55	0.57	0.58	0.00	21.48
P101_A1	Vio	4	-4	mV	-2.78	0.64	3.35	0.46	2.42	-2.39	0.80	3.45	0.52	2.11
P106_*2	lcc	0.9	0.24	mA	0.65	0.68	0.70	0.01	11.16	0.65	0.69	0.70	0.01	11.01
P101_A2	Vio	4	-4	mV	-2.80	0.66	3.41	0.47	2.38	-2.43	0.80	3.49	0.53	2.07
P105_A1	SVR	none	65	dB	103.95	129.15	147.96	8.18	N/A	101.49	127.07	147.96	8.48	N/A
P109_A1	cmr	none	65	dB	92.40	101.71	149.10	3.10	N/A	94.50	105.51	149.10	6.59	N/A
P104_A1	Avd	none	50	V/mV	166.59	415.15	10000.00	248.29	N/A	101.70	374.76	1780.87	65.03	N/A
P117_A4	Vol	0.015	none	V	0.00	0.00	0.00	0.00	54.60	0.00	0.00	0.00	0.00	57.67
P117_A3	Voh	none	3.5	V	3.76	3.77	3.80	0.01	10.78	3.56	3.58	3.60	0.01	4.70
P117_A2	Voh	none	26	V	28.73	28.74	28.77	0.01	113.90	28.08	28.10	28.12	0.01	102.79
P137A1	Isk	28	10	mA	17.19	17.83	18.04	0.11	23.60	18.49	18.94	19.39	0.09	32.84
P137_A1	Isr	-20	-56	mA	-33.37	-32.81	-31.80	0.22	19.21	-34.54	-34.21	-33.40	0.13	36.80
P137_A2	Isk	0.1	0.012	mA	0.07	0.07	0.08	0.00	11.78	0.07	0.07	0.08	0.00	11.26
P121_A1	GBP	1.12	0.48	MHz	0.73	0.80	0.84	0.01	7.39	0.86	0.89	0.92	0.01	8.27
P113_A1	SRn	0.8	0.24	V/uS	0.25	0.31	0.33	0.01	2.11	0.53	0.54	0.56	0.01	16.71
P113_A1	SRp	0.8	0.24	V/uS	0.48	0.51	0.54	0.01	15.15	0.47	0.49	0.52	0.01	12.39

CMR, SVR, AVD and IIB parameters are non gaussians , so no CPK calculation made.

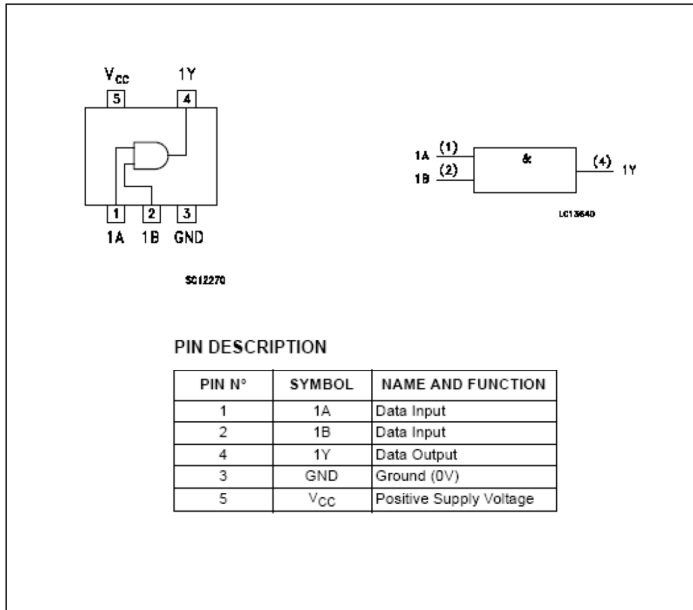
5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.

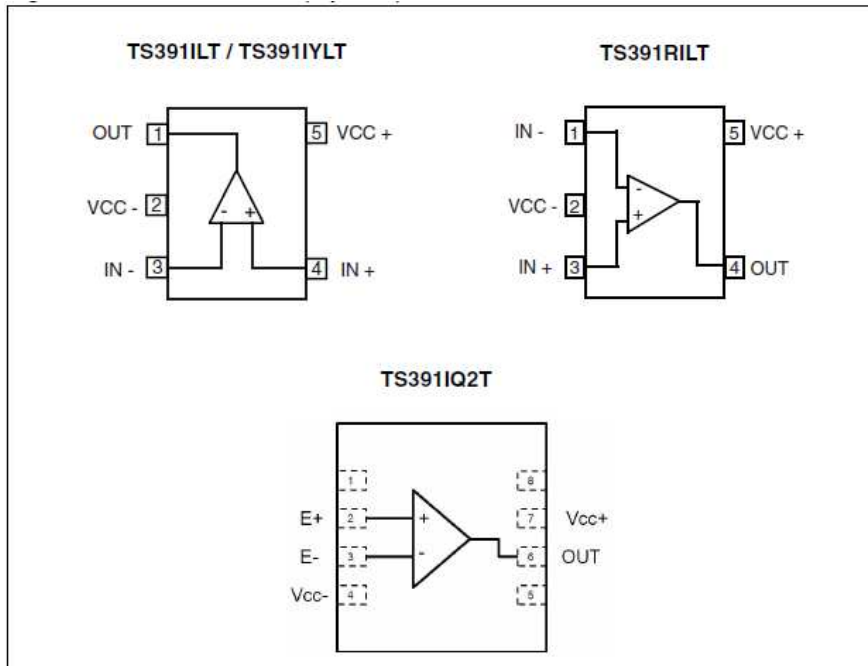
6 ANNEXES:

6.1 Device details

VG08

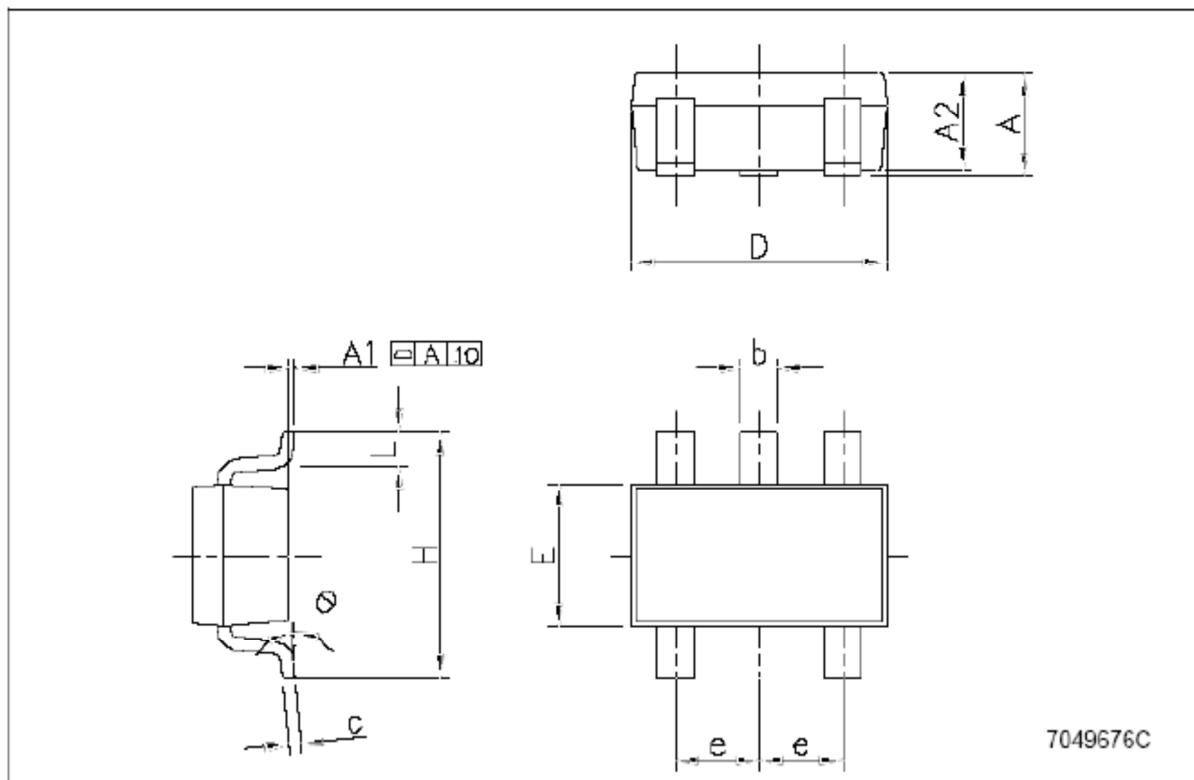


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6.2 Package outlines

SOT23-5L MECHANICAL DATA						
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



6.3 Mechanical data

P/N VG08

Test	Parameter		Specification		Results				Note
	Symbol	Unit	LSL	USL	Min	Avg	Max	Cpk	
WBS	Ball shear	20	15g		26.13	29.6	36.12	1.71	
WBP	Pull Force	20	4g		9.45	10.9	13.16	2.18	