PRODUCT INFORMATION LETTER

PIL MMS-MIC/12/7220
Notification Date 04/13/2012

STM32F20x, STM32F21x Low Speed Oscillator consumption decrease

Production process involved	Product design change
Production process details	Generic
Reason for change	Decrease Low Speed Oscillator consumption for low power applications
Description	On revX devices, the power consumption of the Low Speed Oscillator (32.678KHz Real Time Clock) has been reduced from 3 A to 1 A at typical conditions (VDD=3.3Volts and 25 C), thus providing better current consumption in VBAT mode while keeping the Low Speed Oscillator and Real Time Clock active for low power applications.
Forecasted date of implementation	05-May-2012
Forecasted date of samples for customer	06-Apr-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	06-Apr-2012
Description of qualification program	See Attached Qualification Plan
Involved ST facilities	ST Rousset diffusion plant

DOCUMENT APPROVAL

Name	Function
Colonna, Daniel	Division Marketing Manager
Narche, Pascal	Division Q.A. Manager
Delannoy, Alain	Process Owner

PRODUCT INFORMATION LETTER

STM32F20x, STM32F21x
Low Speed Oscillator consumption decrease

MMS - Microcontrollers Division (MCD)

Dear Customer,

We wish to inform you about an improvement related to the Low Speed Oscillator on STM32F20x and STM32F21x devices.

What is the change?
On revX devices, the power consumption of the Low Speed Oscillator (32.678KHz Real Time Clock) has been reduced from 3µA to 1µA at typical conditions (VDD=3.3Volts and 25°C), thus providing better current consumption in VBAT mode while keeping the Low Speed Oscillator and Real Time Clock active for low power applications.

Why?
The power consumption of the Low Speed Oscillator of the Real Time Clock is reduced by factor of 3 at typical conditions, which is perfect for low power applications.

When?
The design improvement will be implemented week 18.

How will the change be qualified?
This change is already qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard.

Qualification plan

See Qualification plan attached at the end of this document.

What is the impact of the change?

ST decreased the power consumption on VBAT from 3µA to 1µA (25°C and 3.3volts), while keeping the same functionality for the Low Speed Oscillator in terms of oscillations and all other features.

BEFORE:

Table 21. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions	Typ		
			T_A = 25 °C		
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, RTC ON	3.2	3.4	3.7
		Backup SRAM OFF, low-speed oscillator and RTC ON	2.6	2.7	3.0
		Backup SRAM ON, RTC OFF	0.7	0.7	0.8
		Backup SRAM OFF, RTC OFF	0.1	0.1	0.1

NOW:

Symbol	Parameter	Conditions	Typ		
			T_A = 25 °C		
			V_{BAT} = 1.8 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10

How can the change be seen?

Traceability of the change is ensured by ST internal tools.

• The new revision letter of the die is changed from **"Y" to "X".** The die revision is marked onto the package of the part.

• The Finish good identification is changed from 32F2xxxx$x4 to 32F2xxxx$x5. The Finish good identification is printed onto the labels of the inner box and outer box.

We remain available for any complementary information you may need concerning this change.

With our sincere regards.

Michel Buffa
Microcontroller Division General Manager

MMS/MCD RELIABILITY EVALUATION REPORT

RERMCD1023

Product Evaluation: STM32F20x / 1M

CMOSM10 ST Rousset

Product / Process information	
Commercial product	STM32F2x
Product line	411X66
Product description	STM32F 1Mbytes FLASH
Production Mask Set revision	Cut 2.2
Product Division	Microcontrollers Division (MCD)
Silicon process technology	CMOSM10
Wafer fabrication location	R8", ST Rousset, France
Electrical Wafer Sort test plant location	R8", ST Rousset, France

Package information		
Package	**Assembly Plant location**	**Final Test plant location**
LQFP 176 (24x24)	ASE (TAIWAN)	ST MUAR, (MALAYSIA)
LQFP 144 (20x20)	AMKOR ATK1 (KOREA)	AMKOR ATK3 (KOREA)
LQFP 100 (14x14)	AMKOR ATK1 (KOREA)	AMKOR ATK3 (KOREA)
LQFP 64 (10x10)	STATS ChipPAC (SHANGHAI)	STATS ChipPAC (SHANGHAI)
UFBGA 176 (10x10)	AMKOR ATK4 (KOREA)	AMKOR ATK3 (KOREA)
WLCSP66	STATS ChipPAC Singapore	STATS ChipPAC Singapore

Reliability assessment: PASS

Approval List		
Function	**Name**	**Date**
Div Q&R Responsible	Frederic BRAVARD	05-April-2012
Div Quality Manager	Pascal NARCHE	05-April-2012

Contents

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

The purpose of this document is to assess the reliability of the product STM32F20x diffused in STM Rousset, France, and assembled in the following package:

- For LQFP176 24x24 in ASE, Taiwan
- For LQFP144 20x20 in AMKOR ATK1, Korea
- For LQFP100 14x14 in AMKOR ATK1, Korea
- For LQFP64 10x10 in STATS ChipPAC Shanghaï, China
- For WLCSP66 in STATS ChipPAC Singapore
- For UFBGA176 10x10 in AMKOR ATK4, Korea.

1.2 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to the reliability tests results, the qualification is granted for the STM32F20x F/G and its subsets, diffused in STM Rousset R8" – France (die 411X) and assembled in the above listed packages.

The intermediate results of WLCSP66 reliability trials are enough to grant production maturity.
The report will be updated when the full trial will be completed.

2 RELIABILITY TEST VEHICLE(S) CHARACTERISTICS

2.1 Reliability Test vehicle(s) description

STM32F20x is processed in CMOSM10 (90nm) diffused in ROUSSET 8". The test vehicle used for the die reliability evaluation is assembled in LQFP176 24x24 package. The reliability evaluation has been also performed for the following packages: LQFP176 24x24, LQFP144 20x20, LQFP100 14x14 and LQFP64 10x10.
UFBGA176 10x10
WLCSP66

The STM32F20x family is based on the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a frequency of up to 120 MHz. The family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 128 Kbytes of system SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The devices also feature an adaptive real-time memory accelerator (ART Accelerator™) which allows to achieve a performance equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz. This performance has been validated using the CoreMark benchmark.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. A true number random generator (RNG). They also feature standard and advanced communication interfaces. New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), and a camera interface for CMOS sensors.

The devices also feature standard peripherals:

- Up to three I2Cs
- Three SPIs, two I2Ss. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external PLL to allow synchronization.
- 4 USARTs and 2 UARTs
- An USB OTG full-speed and a USB OTG full-speed with high-speed capability (with the ULPI)

2.2 Reliability Test vehicle(s) Traceability

2.2.1 Product vehicle used for die reliability evaluation

RER lot ID	Lot 1	Lot 2	Lot 3	Lot 4	Lot 11
Product	Cut 1.1	Cut 1.1	Cut 2.0	Cut 2.1	Cut 2.2
Lab Location	ST ROUSSET				ST ROUSSET
Wafer fab.	ROUSSET 8”				ROUSSET 8”
Silicon Process Technology	*CMOSM10 (90nm)*				*CMOSM10 (90nm)*
EWS location	ST ROUSSET				ST ROUSSET
Assembly plant location	ASE TAIWAN				AMKOR ATK4
Package description	LQFP176 24x24				UFBGA176 10x10

2.2.2 Product vehicle used for package reliability evaluation

RER lot ID	Lot 5	Lot 6	Lot 7	Lot 8	Lot 9	Lot 8	Lot 9	Lot 10
Product	Cut 2.0	Cut 2.0	Cut 2.0	Cut 2.0	Cut 2.0	Cut 1.1	Cut 1.1	Cut 2.0
Lab Location	ST ROUSSET							
Wafer fab.	ROUSSET 8”							
Silicon Process Technology	*CMOSM10 (90nm)*							
EWS location	ST ROUSSET							
Assembly plant location	STATS ChipPAC Singapore					AMKOR ATK1	AMKOR ATK1	STATS ChipPAC Shanghaï
Package description	WLCSP66					LQFP144 20x20	LQFP100 14x14	LQFP64 10x10

3 RELIABILITY EVALUATION PLAN / RESULTS SUMMARY

3.1 Reliability evaluation : results summary

The STM32F20x is a new platform for the 32 bits microcontroller processed in the CMOSM10 (90nm) with embedded Flash memory. This technology is qualified in ST Rousset.

For packages used on STM32F20x, the following rules have been applied:

- Full similarity rules: LQFP144, LQFP100 and LQFP64
- Full qualification package: LQFP176, UFBGA176, WLCSP66

Packages qualification references:

Package	Qualification Report	Assembly Plant location	Final Test plant location
LQFP176 24x24	RERMCD 1023	ASE TAWAIN	ST MUAR
LQFP144 20x20	RERMCD 1018	AMKOR ATK1	AMKOR ATK3
LQFP100 14x14	UFBGA176	AMKOR ATK1	AMKOR ATK3
LQFP64 10x10	QA 08-005	SCC	SCC
UFBGA176	RERMCD 1108	AMKOR ATK4	AMKOR ATK3
WLCSP66	RERMCD 1023	StatsChippac Singapore	StatsChippac Singapore

Based on these data, the following qualification strategy has been defined:

- Minimum of 3 diffusion lots (-40℃ / +105℃)

The reliability test plan and result summary are presented as follows:

- In ***Table 1*** for Die oriented tests
- In ***Table 2*** for LQFP176 package oriented tests
- In ***Table 3*** for LQFP144 package oriented tests
- In ***Table 4*** for LQFP100 package oriented tests
- In ***Table 5*** for LQFP64 package oriented tests
- In ***Table 6*** for WLCSP66 package oriented tests

3.1.1 Die related tests:

The die oriented test results are summarized in table 1.

Table 1. Die oriented test results

	Die Related Tests - short description					Results				
Description	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Read out / Duration***	***Lot 1***	***Lot 2***	***Lot 3***	***Lot 4***	***Lot 11***
						Cut 1.1	Cut 1.1	Cut 2.0	Cut2.1	Cut2.2
Electrostatic discharge - Human Body Model										
ESD HBM	JESD22-A114	1500 Ω, 100 pF	3 x 3	2kV 1KV on VBAT domain Class 2	2kV 1KV on VBAT domain		0/3	0/3	0/3	0/3
Electrostatic discharge - Charge Device Model										
ESD CDM	JESD22-C101	LQFP176	1 x 3	500V class II	500V		0/3	0/3	0/3	0/3
		UFBGA176	1 x 3				0/3			0/3
		LQFP144	1 x 3				0/3			W15-12
		LQFP100	1 x 3				0/3			W15-12
		LQFP64	1 x 3					0/3		W12-12
		WLCSP66	1x3					0/3		W21-12
LATCH UP										
LU	JESD78	LQFP176	3 x 6	A0/R1	125℃		0/6	0/6	0/6	0/6
NVM Endurance & Data Retention – 10kcy EW @ +125℃ then Storage										
EDR	JESD-22A117	HTB 175℃	3 x 77	A0/R1 10kcyc + 672h	72h	0/77	0/77	0/77		
					336h	0/77	0/77	0/77		
					672h	0/77	0/77	0/77		
NVM Endurance & Data Retention – 10kcy EW @ +25℃ then Storage										
EDR	JESD-22A117	HTB 175℃	2 x 77	A0/R1 10kcyc + 72h	72h			0/77	0/77	
NVM Endurance & Data Retention – 10kcy EW @ +-40℃ then Storage										
EDR	JESD-22A117	HTB 175℃	1 x 77	A0/R1 10kcyc + 72h	72h				0/77	
Early Life Failure Rate										
ELFR	MIL-STD-883 Method 1005 JESD22-A108 JESD74	HTOL 140℃, 3v3	3 x 500	A0/R1 24h	24h	0/500	0/500	0/500		
High Temperature Operating Live										
HTOL	JESD-22A108	HTOL 140℃, 3v3	3 x 77	A0/R1 672h	72h	0/77	0/77	0/77		
					168h					0/77
					336h	0/77	0/77	0/77		
					672h	0/77	0/77	0/77		

3.1.2 Packages related tests:

The package oriented test results are summarized in the following tables.

*Table 2. **LQFP176** package oriented test results*

Short description						Results		
Descript.	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Read out /Duration***	***Lot 1***	***Lot 2***	***Lot 3***
						Cut 1.1	Cut 1.1	Cut 2.0
Preconditioning: moisture sensitivity level 3								
PC	J-STD-020D JESD22-A113	Peak temperature at 260 ℃, 3 IR-reflows	1 x 308	A0/R1	N.A	0/308	0/308	0/308
Temperature Humidity Bias after Preconditioning								
THB	JESD 22-A101	85℃, 85% RH	1 x 77	A0/R1 1000h	500h	0/77	0/77	0/77
					1000h	0/77	0/77	0/77
Autoclave after Preconditioning								
AC	JESD 22-A102	Ta=121℃ P=2.08atm	1 x 77	A0/R1 96h	96h	0/77	0/77	0/77
Thermal Cycling after Preconditioning								
TC	JESD 22-A104	Ta=-50℃/+150℃	1 x 77	A0/R1 1000TC	500 TC	0/77	0/77	0/77
					1000 TC	0/77	0/77	0/77
High Temperature Storage Life after Preconditioning								
HTSL	JESD 22-A103	150℃	1 x 77	A0/R1 1000h	500h	0/77	0/77	0/77
					1000h	0/77	0/77	0/77

*Table 3. **LQFP144** package oriented test results*

Short description						Results
Descript.	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Read out /Duration***	***Lot 8***
						Cut 1.1
Preconditioning: moisture sensitivity level 3						
PC	J-STD-020D JESD22-A113	Peak temperature at 260 ℃, 3 IR-reflows	1 x 308	A0/R1	N.A	0/308
Temperature Humidity Bias after Preconditioning						
THB	JESD 22-A101	85℃, 85% RH	1 x 77	A0/R1 1000h	500h	0/77
					1000h	0/77
Autoclave after Preconditioning						
AC	JESD 22-A102	Ta=121℃ P=2.08atm	1 x 77	A0/R1 96h	96h	0/77
Thermal Cycling after Preconditioning						
TC	JESD 22-A104	Ta=-50℃/+150℃	1 x 77	A0/R1 1000TC	500 TC	0/77
					1000 TC	0/77
High Temperature Storage Life after Preconditioning						
HTSL	JESD 22-A103	150℃	1 x 77	A0/R1 1000h	500h	0/77
					1000h	0/77

*Table 4. **LQFP100** package oriented test results*

Short description						Results
Descript.	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Read out /Duration***	***Lot 9***
						Cut 1.0
Preconditioning: moisture sensitivity level 3						
PC	J-STD-020D JESD22-A113	Peak temperature at 260 ℃, 3 IR-reflows	1 x 308	A0/R1	N.A	0/308
Temperature Humidity Bias after Preconditioning						
THB	JESD 22-A101	85℃, 85% RH	1 x 77	A0/R1 1000h	500h	0/77
					1000h	0/77
Autoclave after Preconditioning						
AC	JESD 22-A102	Ta=121℃ P=2.08atm	1 x 77	A0/R1 96h	96h	0/77
Thermal Cycling after Preconditioning						
TC	JESD 22-A104	Ta=-50℃/+150℃	1 x 77	A0/R1 1000TC	500 TC	0/77
					1000 TC	0/77
High Temperature Storage Life after Preconditioning						
HTSL	JESD 22-A103	150℃	1 x 77	A0/R1 1000h	500h	0/77
					1000h	0/77

*Table 5. **LQFP64** package oriented test results*

Short description						Results
Descript.	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Read out /Duration***	***Lot 10***
						Cut 1.0
Preconditioning: moisture sensitivity level 3						
PC	J-STD-020D JESD22-A113	Peak temperature at 260 ℃, 3 IR-reflows	1 x 308	A0/R1	N.A	0/308
Temperature Humidity Bias after Preconditioning						
THB	JESD 22-A101	85℃, 85% RH	1 x 77	A0/R1 1000h	500h	0/77
					1000h	0/77
Autoclave after Preconditioning						
AC	JESD 22-A102	Ta=121℃ P=2.08atm	1 x 77	A0/R1 96h	96h	0/77
Thermal Cycling after Preconditioning						
TC	JESD 22-A104	Ta=-50℃/+150℃	1 x 77	A0/R1 1000TC	500 TC	0/77
					1000 TC	0/77
High Temperature Storage Life after Preconditioning						
HTSL	JESD 22-A103	150℃	1 x 77	A0/R1 1000h	500h	0/77
					1000h	0/77

*Table 6. **WLCSP66** package oriented test results*

Short description						Results				
Descript.	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Read out /Duration***	***Lot 5***	***Lot 6***	***Lot 7***	***Lot 8***	***Lot 9***
Temperature Humidity Bias										
THB	JESD 22-A101	85℃, 85% RH	3 x 77	A0/R1 1000h	500h			0/77	0/77	0/77
					1000h			0/77	0/77	*W15-12*
Thermal Cycling										
TC	JESD 22-A104	Ta=65℃/+150℃	2 x 77	A0/R1 500TC	250 TC				0/77	
					500 TC				0/77	0/77
High Temperature Storage Life										
HTSL	JESD 22-A103	150℃	3 x 77	A0/R1 1000h	500h	0/77	0/77	0/77		
					1000h	0/77	0/77	0/77		

4 APPLICABLE AND REFERENCE DOCUMENTS

- ADCS 0061692 : RELIABILITY TESTS AND CRITERIA FOR QUALIFICATIONS
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A117: Endurance and Data retention
- JESD22-C101: Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 GLOSSARY

EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
HTB	High temperature bake
ESD	HBM Electrostatic discharge (human body model)
ESD	CDM Electrostatic discharge (charge device model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
AC	Autoclave (pressure pot)
HTSL	High temperature storage life

6 REVISION HISTORY

Date	Revision	Changes
15-April-2011	1	Initial release.
30-September-2011	2	WLCSP66 intermediate trials reliability results
16-December-2011	3	WLCSP66 intermediate trials reliability results updated
20-December-2011	4	Correction Typo error in Package Qualification references
05-March-2012	5	Adding of Cut 2.2 reliability trials results
06-March-2012	6	Correction Typo error: Cut 2.1 corrected by Cut 2.2 and 411Y corrected by 411X
05-April-2012	7	Update of WLCSP66 reliability trial results

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