



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-IPC/12/7366
Dated 31 Jul 2012

L6591 : METAL MASK CHANGE

Table 1. Change Implementation Schedule

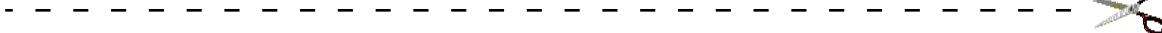
Forecasted implementation date for change	15-Sep-2012
Forecasted availability date of samples for customer	24-Jul-2012
Forecasted date for STMicroelectronics change Qualification Plan results availability	24-Jul-2012
Estimated date of changed product first shipment	15-Jan-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	L6591 and L6591TR
Type of change	Product design change
Reason for change	To enhance burst mode functionality.
Description of the change	We have added the thermal compensation of the two diodes (2 Vbe) attached to the COMP pin. We have also modified the Icomp minimum limit.
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN IPD-IPC/12/7366	
Please sign and return to STMicroelectronics Sales Office		Dated 31 Jul 2012	
<input type="checkbox"/> Qualification Plan Denied	Name:		
<input type="checkbox"/> Qualification Plan Approved	Title:		
	Company:		
<input type="checkbox"/> Change Denied	Date:		
<input type="checkbox"/> Change Approved	Signature:		
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DOCUMENT APPROVAL

Name	Function
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Motta, Antonino	Q.A. Manager



WHAT:

We have added the thermal compensation of the two diodes (2 Vbe) attached to the COMP pin. We have also modified the Icomp minimum limit.

WHY:

To improve the burst mode performance and to maximize the yield.

HOW:

Through a metal mask change, as per the attached Reliability Report.

This modification will be identified by a new internal part number :

L6591-6LF/

L6591TR-6LF/

WHEN:

The production of the new product will be based on material availability and customers' volumes. Phase-out and phase-in will be done accordingly.

Samples of the new product are already available.

Reliability Report

General Information	
Product Line	<i>MU62BBX(UL25CB5+U335AB6)</i>
Product Description	<i>PWM CONTROLLER FOR ZVS HALF-BRIDGE</i>
Product division	<i>I&PC</i>
Package	<i>SO16N</i>
Silicon process technology	<i>BCD6 (UL25) – BCDoffline(U335)</i>

Locations	
Wafer fab location	<i>CATANIA(UL25) + ANG MO KIO(U335)</i>
Assembly plant location	<i>AMKOR ATP1 - PHILIPPINES</i>
Reliability assessment	<i>Pass</i>

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	4-July -12	7	G. Capodici	Original document

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of MU62BBX(UL25CB5+U335AB6) device diffused in CATANIA(UL25) + ANG MO KIO(U335) and assembled in SO16N in AMKOR ATP1 - PHILIPPINES.

The MU62 BBX device is a metal option of the already qualified MU62 BAX device (See RR007709CS2047). According to Reliability Qualification Plant, below is reported the electrical characterization:

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the trials performed the **MU62BBX(UL25CB5+U335AB6) diffused in CATANIA(UL25) + ANG MO KIO(U335) and assembled in SO16N in AMKOR ATP1 - PHILIPPINES can be qualified** from reliability viewpoint.

3 DEVICE CHARACTERISTICS

3.1 Traceability

Wafer fab information (UL25)	
Wafer fab manufacturing location	CATANIA
Wafer diameter	8 inches
Wafer thickness	375 μ m
Silicon process technology	BCD6
Die finishing back side	Raw Silicon
Die size	1373x1058 μ m
Bond pad metallization layers	AlCu
Passivation	USG+SiN+Polyimide
Metal levels	3

Wafer fab information (U335)	
Wafer fab manufacturing location	ANG MO KIO
Wafer diameter	6 inches
Wafer thickness	375 μ m
Silicon process technology	BCD OFFLINE
Die finishing back side	Cr/Ni
Die size	1930x2020 μ m
Bond pad metallization layers	AlSiCu
Passivation	SiN
Metal levels	1

Assembly Information	
Assembly plant location	AMKOR ATP1 - PHILIPPINES
Package description	SO16N
Die pad size	2.438x4.826mm
Molding compound	Sumitomo G600
Wires bonding materials/diameters	Au/1mils
Die attach material	Ablebond 8290
Lead solder material	Sn

4 TESTS RESULTS SUMMARY LATCH-UP

4.1 Test plan and results summary

Electrical Characterization Tests						
Test	Method	Conditions	Sample/ Lots	Number of lots	Duration	Results Fail/SS
ESD	Electro Static Discharge					
	Human Body Model	+/- 2kV ALL pins except HV (13,14,15,16) pins +/- 1kV Only HV (13,14,15,16) pins	3	1		0/3
	Charge Device Model	+/- 750V	3	1		0/3
LU	Latch-Up					
	Over-voltage and Current Injection	Tamb=85°C Jedec78	6	1		0/6

5 ELECTRICAL CHARACTERIZATION TESTS

5.1.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up. The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

The latch up test was performed in the two following conditions:

1. Pin1 max current 1mA, Pin 8 max current 3mA, Pins 12-16 NC, Pins 1,2,3,4 always LOW, tested only negative trials
2. Pin1 max current 1mA, Pin8 max current 3mA, Pins 12-16 NC, Pins 1, 2 always HIGH, tested only positive trials, Pins 3, 4 always LOW, tested only negative trials

In both cases the device passes Injection Negative up to -50mA and Injection Positive up to +100mA, and Overvoltage up to 25V.

5.1.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.

The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** ANSI/ESDA/JEDEC STANDARD JES001
CDF-AEC-Q100-002
- **Charge Device Model** ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
CDF-AEC-Q100-011

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