PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-APD/12/7237
Notification Date 04/20/2012

Material set change for SO8, SO14 & SO16 packages

produced in ST Bouskoura (Morocco)

Table 1. Change Implementation Schedule

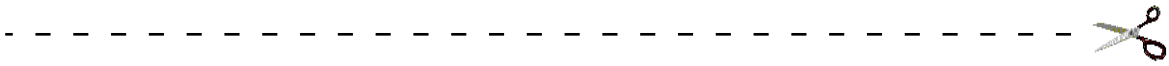
Forecasted implementation date for change	13-Apr-2012
Forecasted availabillity date of samples for customer	13-Apr-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	13-Apr-2012
Estimated date of changed product first shipment	20-Jul-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Multiple types of changes
Reason for change	Production rationalization
Description of the change	Progressing on the activities related to SO manufacturing processes, ST is glad to announce availability of a new material set halogen free, for Analog Division of AMS Group products assembled in SO8-14-16 packages in ST Bouskoura (Morocco) plant. Samples availability: week 21 2012. If requested by customer, please enter in the system a non-standard samples order in class 2 with comment "PCN#7174 qualification". Then send an e-mail to Angelique DUCHENE with SO# for availability follow-up. 1st shipment timeschedule: for products assembled in SO8 & SO16 ==> June 2012. For products assembled in SO14 ==> August 2012.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	On label 2nd level interconnect digit does change from E4 ==> E3
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN AMS-APD/12/7237**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 04/20/2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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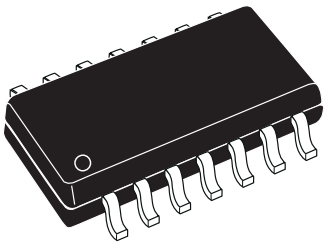
DOCUMENT APPROVAL

Name	Function
Camiolo, Jean	Division Marketing Manager
Grillo, Lionel	Division Marketing Manager
Lefebvre, Laurence	Division Marketing Manager
Mcdonagh, Gary	Division Marketing Manager
De marco, Alberto	Division Product Manager
Italia, Francesco	Division Product Manager
San biagio, Marcello	Division Product Manager
Bugnard, Jean-Marc	Division Q.A. Manager
Lisi, Giuseppe	Division Q.A. Manager

Analog, MEMS and Sensor Group

New material set halogen free for SO Narrow produced in ST Bouskoura (Morocco)



SO Narrow

WHAT:

Progressing on the activities related to SO manufacturing processes, ST is glad to announce availability of a new material set halogen free, for AMS products produced in SO.

Material	Current process SO8/14/16	Modified process SO8/14/16
Assembly location	ST Bouskoura	ST Bouskoura
Die attach	ABLEBOND 8601S-25	ABLEBOND 8601S-25
Wire	Copper 1 mil	Copper 1mil
Leadframe	Copper	Copper
Plasma cleaning	Yes	Yes
Plating	**NiPdAgAu**	**Sn**
Molding compound	**Sumitomo G700K**	**Sumitomo EME G630AY**

For the complete list of the part numbers affected by the change, please refer to the attached Products list.
Samples will be available upon request from W221.

WHY:
To internalize plating process for better control, to improve product reliability and performance through molding compound change (see below table) for SO packages produced in ST Bouskoura.

	current compound	New compound	Comment
Tg (°C)	125	135	
CTE1 (10^{-5}/°C)	1.2	0.9	Better matched with silicon CTE which will reduce mechanical stress during thermal variation, reducing delamination risk and reducing electrical drift caused by piezoelectrical effect.
CTE2 (10-5/°C)	4.9	3.4	
F. modulus at 25°C (N/mm²)	19000	25000	Stiffer compound allowing less package deformation and then minimizing stress on die.
F. modulus at 260°C (N/mm²)	600	700	
Cl- (ppm)	4	2	Less ionic contamination which is important for Copper bonding.
Water absorption	0.15	0.13	Little reduction of water absorption minimizing water content inside package and then reducing stress during package soldering

HOW:
The change, that covers AMS products, is under qualification through attached qualification plan. Here below you'll find the details of qualification plan and intermediate results.

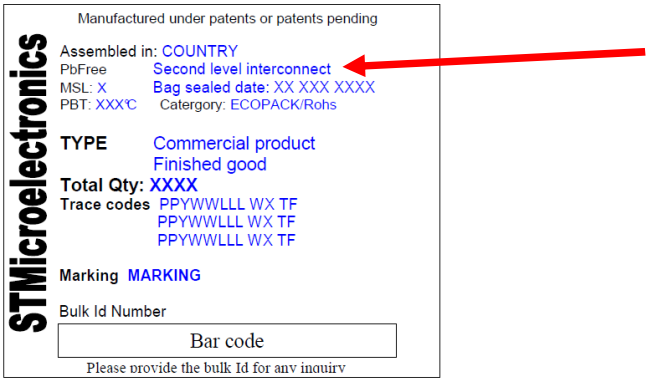
Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

WHEN:
Production in ST Bouskoura for AMS is forecasted in June 2012 for SO8/S016 and in August 2012 for S014.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales types and marking on package and on label.
2nd level interconnect will move from e4 to e3.



The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Reliability Report

New Halogen free material set SO
ST Bouskoura

General Information	
Product Line	*0912, 0393, 0924, P60B*
Product Description	Dual Op amp CMOS, Dual op amp bipolar, Rail to rail op amp, ripple carry binary counter/divider and oscillator
P/N	*TS912IDT, LM393DT, TS924IDT, HCF4060M013TR*
Product Group	*AMS*
Product division	*Analog*
Package	*SO8/14/16*
Silicon Process technology	*CMOS HC1PA, HBIP40, HF2CMOS, CMOS metal gate*

Locations	
Wafer fab	*ST Singapore*
Assembly plant	*ST Bouskoura (Morocco)*
Reliability Lab	*Grenoble*

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify new material set for SO produced in ST Bouskoura for AMS (Analog Mems & Sensor) group

3.2 Conclusion

Qualification Plan requirements have been fulfilled, up to now, without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

***TS912IDT*:** The TS912 is a rail-to-rail CMOS dual operational amplifier designed to operate with a single or dual supply voltage. The input voltage range V_{icm} includes the two supply rails V_{CC+} and V_{CC-}.
The output reaches V_{CC-} +30 mV, V_{CC+} -40 mV, with R_L = 10 kohms and V_{CC-} +300 mV, V_{CC+} -400 mV, with R_L = 600 ohms**.**
This product offers a broad supply voltage operating range from 2.7 to 16 V and a supply current of only 200 ⌠A/amp (V_{CC} = 3 V).
Source and sink output current capability is typically 40 mA (at V_{CC} = 3 V), fixed by an internal limitation circuit.

***LM393D*:** These devices consist of two independent low voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.
These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

***TS924IDT*:** The TS924 is a rail-to-rail quad BiCMOS operational amplifier optimized and fully specified for 3 and 5 V operation.
High output current allows low load impedances to be driven. The TS924 exhibits a very low noise, low distortion, low offset and high output current capability, making this device an excellent choice for high-quality, low-voltage and battery-operated audio systems.

HCF4060M013TR: The HCF4060B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4060B consists of an oscillator section and 14 ripple carry binary counter stages.
The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which reset the counter to the all 0's state and disable oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi 1$ (and $\phi 0$). All inputs and outputs are fully buffered. Schmitt trigger action on the clock pin permits unlimited clock rise and fall time.

4.2 Construction note

	P/N TS912IDT	**LM393DT**	**P/N TS924IDT**	**P/N *HCF4060M013TR***
Wafer/Die fab. information				
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Technology	CMOS HC1PA	HBIP40	HF2CMOS	CMOS metal gate
Process family	C1PAHV-2	GHBIP40-A	HFMS520	CMOSMG
Die finishing back side	RAW SILICON	LAPPED SILICON	RAW SILICON	LAPPED SILICON
Die size (microns)	2630x1980	870x590	1980x2450	1950x1700
Bond pad metallization layers	AlSi	AlSiCu	AlSiCu	AlSi
Passivation type	P-VAPOX/NITRIDE	P-VAPOX/NITRIDE	P-VAPOX/NITRIDE	P-VAPOX (Si glass)
Wafer Testing (EWS) information				
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information				
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO8	SO14	SO16
Molding compound	EME G630AY	EME G630AY	EME G630AY	EME G630AY
Frame material	Cu	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	Electroplating	Electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	Matte tin
Final testing information				
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	HC1PA/SO8	0912	*CZ2090FV01*
2	HBIP40/SO8	0393	
3	HF2CMOS/SO14	0924	*CZ20607401*
4	Metal gate/SO16	P60B	*CZ2080GV01*

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 1 0912	Lot 2 0393	Lot 3 0924	Lot 3 P60B	
Die Oriented Tests										
HTB	N	JESD22 A-108	Tj = 125°C, BIAS		168 H		0/78	0/78	0/50	
					500 H		0/78	0/78	50	
					1000 H		78	0/78	50	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/77	0/77	0/78	0/77	
					500 H	0/77	0/77	0/78	0/77	
					1000 H	77	77	0/78	77	
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	0/154	0/233	0/234	0/231	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77	0/77	0/78	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/78	0/78	0/77	
					200 cy	0/77	0/78	0/78	0/77	
					500 cy	0/77	0/78	0/78	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H		0/78	0/78	77	
					500 H		0/78	0/78	77	
					1000 H		78	78	77	
Other Tests										
ESD	N	AEC Q101-001, 002 and 005	HBM		2KV					
			CDM		1500V	3	3	3	3	
			MM		150V					
SD	N		After ageing 8h and 16h			0/24	0/24	0/24	0/24	

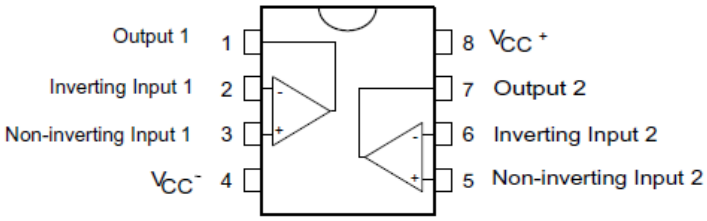
6 ANNEXES

6.1 Device details

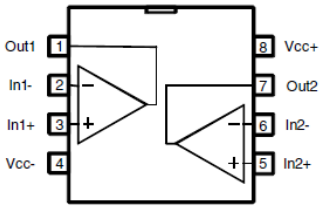
6.1.1 Pin connection

TS912IDT

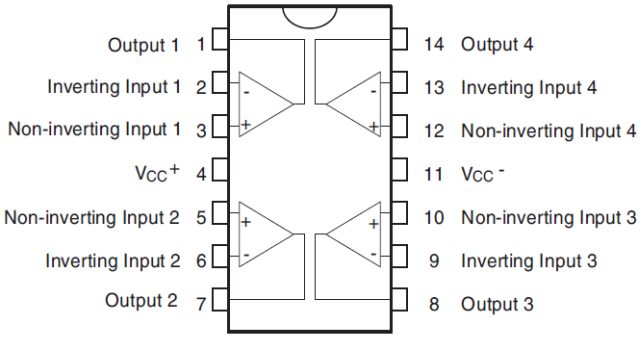
Pin connections (top view)



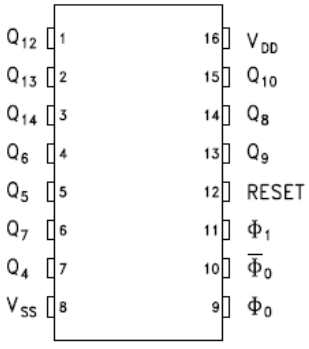
LM393DT



TS924IDT



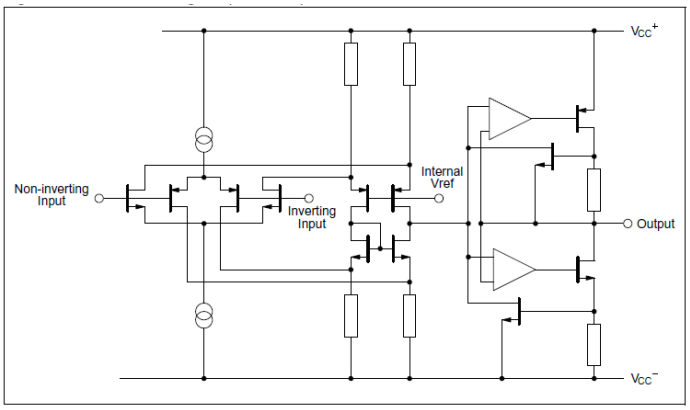
HCF4060M013TR



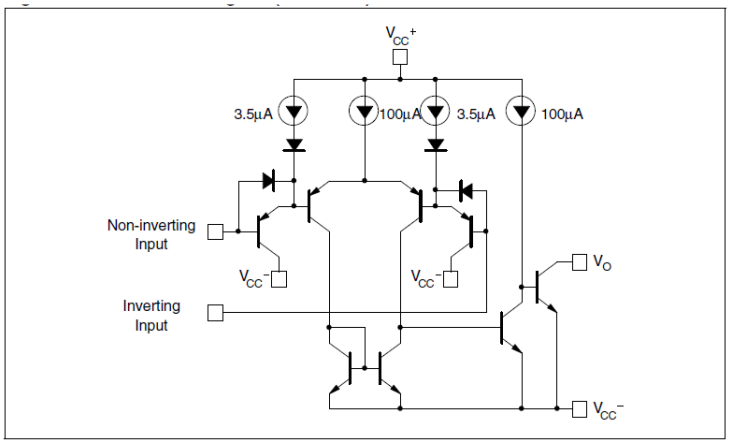
PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 13, 14, 15	Q_{12}, Q_{13}, Q_{14}, Q_6, Q_5, Q_7, Q_4, Q_9, Q_8, Q_{10}	Outputs
9, 10, 11	Φ_0, $\overline{\Phi}_0$, Φ_1	Oscillator Input
12	RESET	Reset
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

6.1.2 Block diagram

TS912IDT



LM393DT



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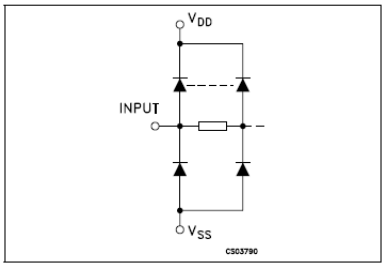

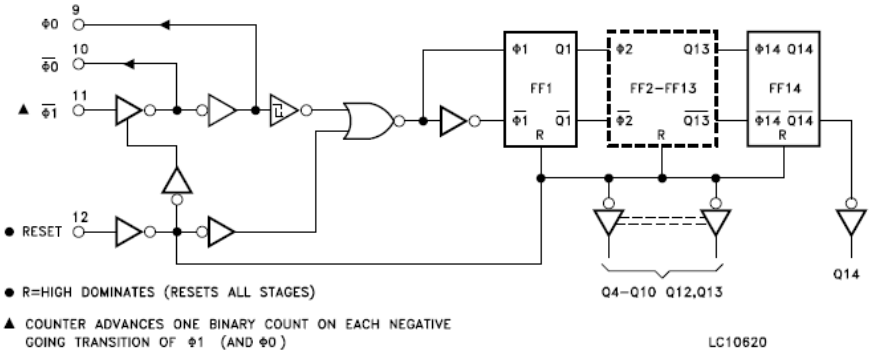

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

6.3 **Additional results**

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<tr><td colspan="2">USL</td><td>NA</td><td>NA</td></tr>
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<table>
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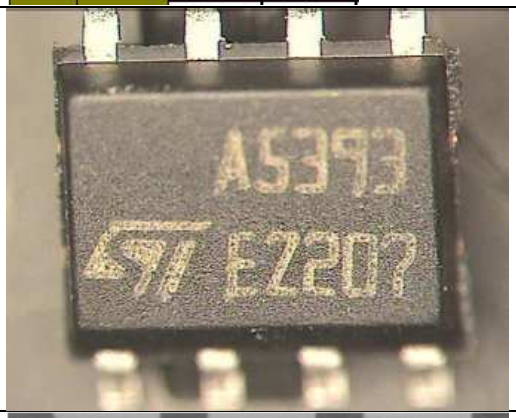
<tr><td>Picture</td><td> 
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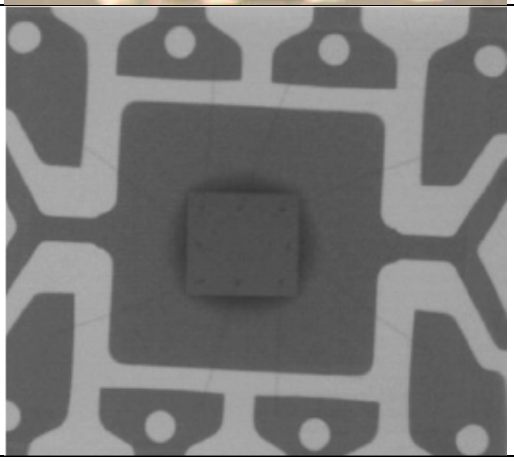
<tr><td>Xray</td><td>  </td><td></td></tr>
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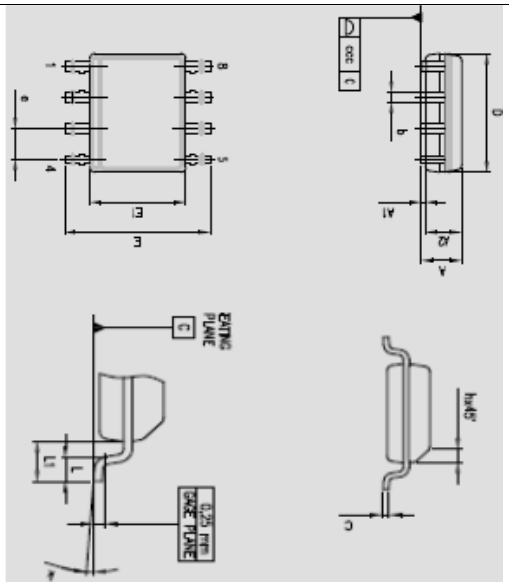
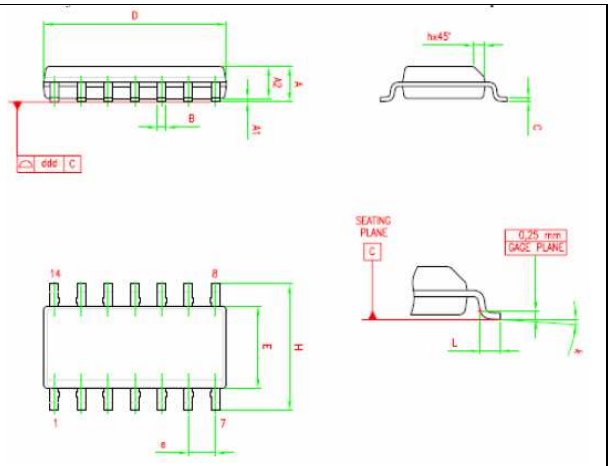
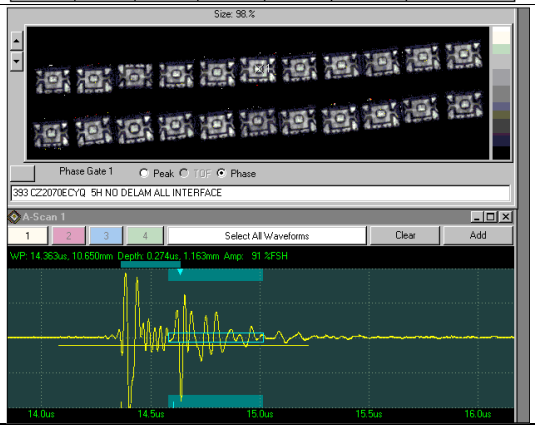


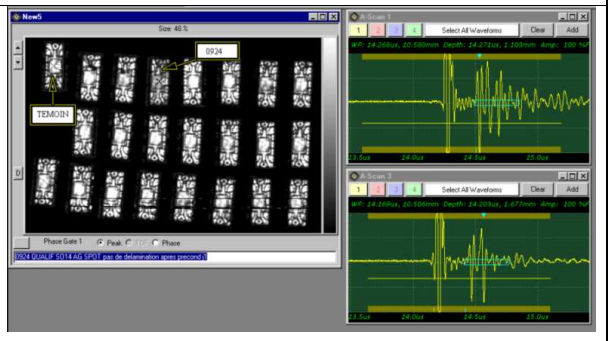
Spec n°0016023						
All values are in mm						
REF	MIN	TYP	MAX	Unit 1	Unit 2	Comment
A			1,75	1,72	1,70	OK
A1	0,10		0,25	0,22	0,20	OK
A2	1,25			1,51	1,51	OK
b	0,28		0,48	0,41	0,40	OK
c	0,17		0,23	0,22	0,17	OK
D	4,80	4,90	5,00	4,82	4,87	OK
E	5,80	6,00	6,20	6,10	6,00	OK
E1	3,80	3,90	4,00	3,82	3,83	OK
e		1,27		1,27	1,27	OK
h	0,25		0,50	0,49	0,45	OK
L	0,40		1,27	0,72	0,70	OK
L1		1,04		1,10	1,06	OK



	Spec n°					
	All values are in mm					
REF DIM	TYP	MIN	MAX	Unit1	Unit2	Comment
A		1.35	1.75	1.40	1.41	OK
A1		0.10	0.25	0.15	0.19	OK
A2		1.10	1.65	1.20	1.24	OK
B		0.33	0.51	0.41	0.39	OK
C		0.19	0.25	0.21	0.20	OK
D		8.55	8.75	8.60	8.64	OK
E		3.80	4	3.90	3.91	OK
H		5.80	6.20	5.90	5.99	OK
H		0.25	0.50	0.31	0.33	OK
L		0.40	1.27	0.56	0.71	

SAM After Precon Jedec level1: no delamination at die/resin interface





SD

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<tr><td>Bonding strength</td><td>
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<tr><th></th><th></th><th>Ball Shear (g)</th><th>Pull Test (g)</th></tr>
<tr><td colspan="2">LSL</td><td>19.9</td><td>4</td></tr>
<tr><td colspan="2">USL</td><td>NA</td><td>NA</td></tr>
<tr><td rowspan="5"></td><td>Avg</td><td>39.15</td><td>15.71</td></tr>
<tr><td>Max</td><td>44.37</td><td>17.08</td></tr>
<tr><td>Min</td><td>36.58</td><td>13.98</td></tr>
<tr><td>stdv</td><td>1.86</td><td>0.96</td></tr>
<tr><td>CPK</td><td>3.43</td><td>4.07</td></tr>
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</td><td>
<table>
<tr><th></th><th></th><th>Ball Shear (g)</th><th>Pull Test (g)</th></tr>
<tr><td colspan="2">LSL</td><td>19.9</td><td>4</td></tr>
<tr><td colspan="2">USL</td><td>NA</td><td>NA</td></tr>
<tr><td rowspan="5">WB3</td><td>Avg</td><td>42.3</td><td>15.11</td></tr>
<tr><td>Max</td><td>48.8</td><td>16.13</td></tr>
<tr><td>Min</td><td>36.6</td><td>14.43</td></tr>
<tr><td>stdv</td><td>2.50</td><td>0.53</td></tr>
<tr><td>CPK</td><td>2.99</td><td>6.99</td></tr>
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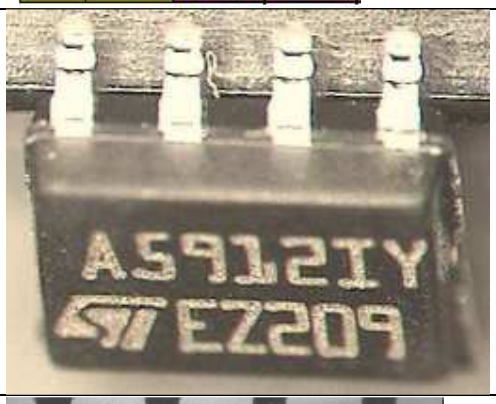
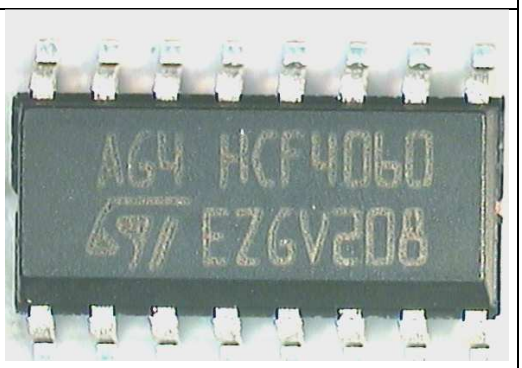
<tr><td>Picture</td><td> 
</td><td> 
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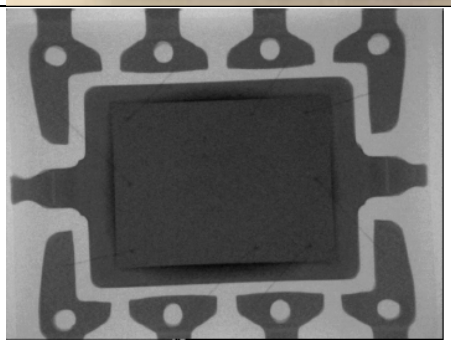
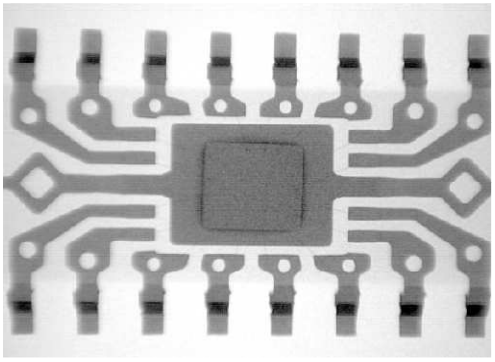
<tr><td>Xray</td><td>  </td><td>  </td></tr>
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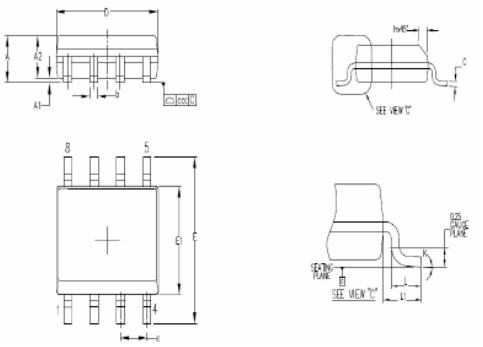
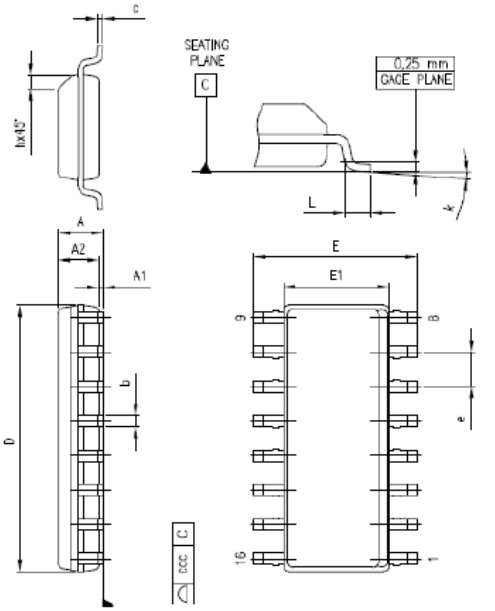
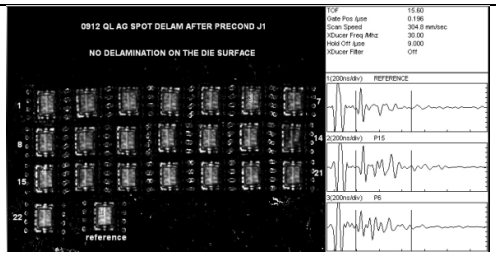


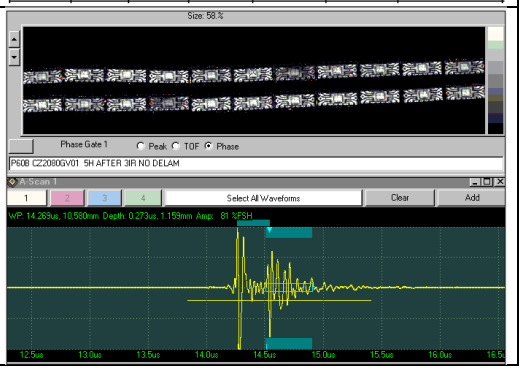
Spec n° 0016023						
All values are in mm						
REF DIM	TYP	MIN	MAX	Unit1	Unit2	Comment
A			1.75	1.2	1.1	OK
A1		0.10	0.25	0.15	0.19	OK
A2		1.25		1.26	1.27	OK
b		0.28	0.48	0.31	0.34	OK
C		0.17	0.23	0.20	0.19	OK
D	4.90	4.80	5.00	4.89	4.88	OK
E	6	5.80	6.20	6.02	6.05	
E1	3.90	3.80	4	3.91	3.89	OK
e	1.27			0.71	0.96	OK
h		0.25	0.50	0.40	0.35	OK
L		0.40	1.27	0.93	0.9	
L1	1.04			1.11	1.01	



Spec n 0016020						
All values are in mm						
REF	MIN	TYP	MAX	Unit 1	Unit 2	Comment
A			1,75	1.65	1.67	OK
A1	0,10		0,25	0,21	0,17	OK
A2	1,25			1,48	1,47	OK
b	0,31		0,51	0,44	0,40	OK
c	0,17		0,25	0,23	0,19	OK
D	9,80	9.90	10,00	9,84	9,87	OK
E	5,80	6.00	6.20	6,05	6,16	OK
E1	3.80	3,90	4.00	3,84	3.87	OK
e		1.27		1.27	1.27	OK
h	0,25		0,50	0,49	0,44	OK
L	0,40		1,27	0.72	0,65	OK

SAM after preconditioning jedec level 1: no delamination at die/resin interface





Electrical comparison:

0912

		Mean Comparison			Cpk comparison			
test	Unit	Old	New	Shift	Old	New	Ratio	Comment
c for one an	mA	0.49	0.50	0.01	1.98	2.74	1.38	
Vio	mV	-0.30	-0.59	-0.29	2.96	3.42	1.15	
Vio	mV	-0.31	-0.73	-0.42	2.94	4.32	1.47	
Icc	uA	0.17	0.17	0.00	2.31	14.79	6.40	
Vio	mV	-0.44	-0.77	-0.34	2.38	4.14	1.74	
Vio	mV	-0.47	-0.99	-0.52	2.38	4.97	2.09	
c for one an	uA	157.34	158.88	1.54	180.00	193.76	1.08	
Iio	pA	0.77	0.98	0.21	13.53	13.89	1.03	
Iio	pA	5.61	2.90	-2.71	20.84	36.92	1.77	

0393

		Mean Comparison			Cpk comparison			
	test parameter	Old	New 68175NT	Shift	Old	New	Ratio	Comment
Limits	0QA 1FT 2WS							
Icc 30V	mA	0.28	0.30	0.02	18.43	22.98	1.25	
Icc 5V	mA	0.24	0.25	0.01	35.08	32.92	0.94	
P101_A1	mV	-0.41	0.07	0.48	6.87	6.17	0.90	
P101_B1	mV	-0.47	-0.28	0.20	4.76	4.74	0.99	
P101_A3	mV	-0.68	-0.29	0.38	6.16	4.59	0.74	CPK>2
P101_B3	mV	-0.71	-0.67	0.05	4.42	3.57	0.81	
P101_A4	mV	0.19	0.56	0.37	6.92	5.60	0.81	
P101_B4	mV	0.13	0.23	0.10	5.15	4.65	0.90	
P101_A2	mV	-0.20	0.25	0.46	7.16	6.26	0.87	
P101_B2	mV	-0.27	-0.07	0.20	4.99	5.07	1.02	
Vol 5V	V	0.25	0.25	-0.67%	5.06	8.66	1.71	
Vol 5V	V	0.25	0.25	0.11%	8.23	9.50	1.15	

0924

		Mean Comparison			Cpk comparison			
test	Units	Old	New	Shift	Old	New	Ratio	Comment
Vio	mV	0.10	0.09	-0.01	8.45	13.39	1.6	
Vio	mV	0.01	0.09	0.08	8.1	10.05	1.2	
Vio	mV	0.04	0.04	0.00	8.23	14.77	1.8	
Vio	mV	0.06	0.09	0.03	7.79	12.16	1.6	
Icc	mA	1.17	1.26	0.09	12.18	18.82	1.5	
Vio	mV	0.05	0.05	0.00	10.22	16.18	1.6	
Vio	mV	0.05	0.06	0.01	9.7	11.67	1.2	
Vio	mV	-0.03	0.03	0.06	9.55	15.65	1.6	
Vio	mV	0.02	0.06	0.03	9.26	13.16	1.4	
Icc	mA	1.02	1.07	0.05	2.88	5.20	1.8	
Vio	mV	0.10	0.09	-0.01	5.00	6.13	1.2	
Vio	mV	0.10	0.10	0.00	3.30	4.41	1.3	
Vio	mV	0.03	0.07	0.04	5.60	6.02	1.1	
Vio	mV	0.06	0.09	0.04	4.10	5.03	1.2	
Icc	mA	0.96	1.01	0.05	4.34	8.41	1.9	
Vio	mV	0.14	0.13	-0.01	4.4	6.09	1.4	
Vio	mV	0.14	0.14	0.00	4.1	4.36	1.1	
Vio	mV	0.07	0.11	0.04	5.2	5.99	1.2	
Vio	mV	0.10	0.13	0.04	4.5	5.01	1.1	

P60B

		Mean Comparison			Cpk Comparison			
Test Name	**Unit**	**Old**	**New**	**% Shift**	**Old**	**New**	**Ratio**	**Comments**
Icc	uA	0.01	-0.03	0.04%	297.49	380.99	1.28	
Icc	uA	0.02	0.01	0.01%	454.59	927.07	2.04	
Icc	uA	0.12	0.07	0.06%	86.45	310.08	3.59	
Icc	uA	0.28	0.02	0.26%	406.38	572.34	1.41	
Vol 5V	mV	131.99	134.77	-2.79%	20.24	31.35	1.55	
Vol 5V	mV	134.09	135.06	-0.97%	18.82	27.32	1.45	
Vol 5V	mV	138.79	137.23	1.56%	18.71	22.77	1.22	
Vol 5V	mV	138.43	137.64	0.79%	18.49	24.04	1.30	
Vol 5V	mV	139.01	137.12	1.88%	18.03	22.66	1.26	
Vol 5V	mV	146.01	144.41	1.60%	17.13	23.07	1.35	
Vol 5V	mV	123.92	126.61	-2.69%	18.06	32.94	1.82	
Vol 5V	mV	141.68	131.88	9.79%	15.75	29.84	1.89	
Vol 5V	mV	148.70	138.11	10.60%	16.96	22.58	1.33	
Vol 5V	mV	157.08	145.93	11.15%	17.21	19.46	1.13	
Vol 15V	mV	217.38	208.10	9.29%	43.32	39.89	0.92	
Vol 15V	mV	386.89	375.07	11.81%	20.05	33.49	1.67	
Vol 15V	mV	403.52	417.17	-13.65%	19.52	26.63	1.36	
Vol 15V	mV	408.17	419.30	-11.14%	19.5	29.90	1.53	
Vol 15V	mV	407.64	416.66	-9.02%	18.35	26.99	1.47	
Vol 15V	mV	420.48	427.56	-7.09%	19.15	27.83	1.45	
Vol 15V	mV	351.04	363.88	-12.84%	21.48	45.69	2.13	
Vol 15V	mV	380.58	393.31	-12.73%	17.21	33.46	1.94	
Vol 15V	mV	415.37	425.96	-10.60%	18.23	26.77	1.47	
Vol 15V	mV	480.26	466.26	14.00%	19.37	22.61	1.17	
Voh 5V	V	4.23	4.24	-0.01%	29.82	23.04	0.77	
Voh 5V	V	4.27	4.24	0.03%	30.4	22.54	0.74	
Voh 5V	V	4.28	4.24	0.04%	33.94	21.22	0.63	
Voh 5V	V	4.27	4.24	0.03%	32.88	18.64	0.57	
Voh 5V	V	4.28	4.24	0.04%	33.19	16.73	0.50	
Voh 5V	V	4.28	4.24	0.04%	33.23	14.54	0.44	
Voh 5V	V	4.26	4.23	0.03%	29.12	12.71	0.44	
Voh 5V	V	4.26	4.25	0.01%	29.23	11.48	0.39	
Voh 5V	V	4.25	4.25	0.00%	26.92	10.81	0.40	
Voh 5V	V	4.24	4.24	0.00%	28.73	11.00	0.38	
Voh 15V	V	14.43	14.31	0.12%	16.22	14.29	0.88	
Voh 15V	V	14.35	14.31	0.05%	16.14	13.52	0.84	
Voh 15V	V	14.36	14.30	0.06%	16.37	11.52	0.70	
Voh 15V	V	14.35	14.30	0.05%	17.37	9.44	0.54	
Voh 15V	V	14.35	14.30	0.06%	16.15	8.00	0.50	
Voh 15V	V	14.35	14.29	0.06%	18.93	6.59	0.35	
Voh 15V	V	14.34	14.28	0.05%	18.42	5.60	0.30	
Voh 15V	V	14.29	14.32	-0.04%	11.84	5.18	0.44	
Voh 15V	V	14.28	14.32	-0.05%	11.92	4.60	0.39	
Voh 15V	V	14.27	14.32	-0.04%	14.25	4.43	0.31	
ILL_pin 11	nA	-19.30	-30.12	10.82%	47.06	6.74	0.14	
ILH_pin 12	nA	-2.69	-4.58	1.89%	750.45	1045.91	1.39	
ILH_pin 11	nA	-12.50	-2.66	-9.84%	108.19	870.66	8.05	
ILL_pin 12	nA	3.94	5.28	-1.35%	260.4	577.85	2.22	

Whiskers test:

Tin Surface Finish Acceptance Testing per JESD201 & JESD 22A121

P.Crema

Assembled :
STM Marocco Bouskoura

SO8L

DISCLAIMER

The whisker test procedures identified in this report are used for determining the presence of tin whiskers and are performed by STMicroelectronics Inc., pursuant to current industry accepted JEDEC standards. The whisker test procedures used herein are unproven and may produce inconclusive results. STMicroelectronics Inc. makes no representation, warranty or guarantee of any kind with respect to the field performance, quality or freedom from whisker-related failures, of any package tested by STMicroelectronics using these procedures.

General Information

Package		**SO8L**
Factory		STMicroelectronics Morocco
Factory Location		Bouskoura
Lead Frame Alloy		Copper : O194
Lead Finish		Matte Tin
Tin Thickness		7 – 20 um on leads
Plating Vendor		Atotech GmbH
Plating Machine		MECO
Plating Chemistry		Stannopure HSM
Mitigation		Post Plating Bake within 24hrs @150 for 1 hr.

Chemical Plating process information

September 11 , 2008					
Description	**Process**	**Volume tank (liter)**	**Make up Concentration (g/l or ml/l)**	**Density**	**Quantity used for the bath**
Electro cleaner	Puronon RTR	80	100g/l		8kg
Activation Ni/Fe					
Activation Cu	Descabase Cu	80	50g/l		4kg
	H2SO4		30ml/l	1.61	3.36litre
Predip	MSA Special Acid HS	80	100ml/l	1.34	8litres
Tin plate	MSA Tin Solution HS 20	320	70g/l	1.53	81 litres
	MSA Special Acid HS		190 g/l	1.34	71 litres
	Stannopure HSM Additive HT		50ml/l	1	16litres
	Stannopure HSM Grain Refiner GF		15ml/l	1	4.8litres
	Antioxydant SN		5ml/l	1	1.6 litres
Neutral	Protectostan LF	80	100ml/l	1	8 litres
Stripper	Becastrip EL Part A	240	550ml/l	1.24	132 litres
	Becastrip EL Part B		20ml/l	1.53	4.8 litres

Plating equipment & process parameters

Equipment identification	Supplier	Type	Model
MECO 1	MECO	Continuous automatic plating	EPL 1200S

	Electro cleaner	Activation	Plating	Neutraliser
Temperature	50°C	RT	45°C	RT
Voltage /Ampérage	50A	30A	120A 120A 120A 120A	-
Belt speed	4.0 m/mn			

Pre Conditions

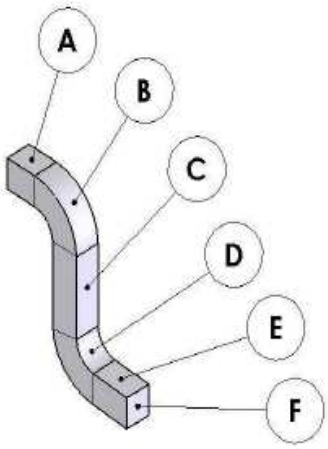
PreCondition	Conditions
No Pre condition	Ambient Only
Reflow (Single Pass)	215 deg C in air
Reflow (Single Pass)	245 – 260 deg C in air

Test plan

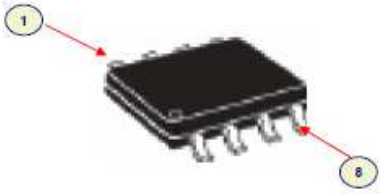
Test	Short description	Conditions
Thermal Cycling	TC	- 40℃ to + 85℃
High Humidity Storage	HT	55℃-85%RH
Controlled Ambient Storarge	RT	30℃-60%RH

Fig 1: Inspection Zones

Inspection: Top + 2 Sides



Lead identification



Temp. Cycles Whiskers inspection results

Optical inspection @ 50 X						
			n. of cycles			
Preconditioning	Device	Sample size	@ 0	@ 500	@1000	@1500
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers
215℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers
247℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers

Soak 30c/60%RH Whisker Inspection Results

Optical inspection @ 50 X							
			Time in hrs				
Preconditioning	Device	Sample size	@ 0	@ 1000	@2000	@3000	@4000
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
215℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
247℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers

Soak 55c/85%RH Whisker Inspection Results

Optical inspection @ 50 X								
			Time in hrs					
Preconditioning	Device	Sample size	@ 0	@ 1000	@2000	@3000	@4000	Discounted lead
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
215℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
247℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--

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