PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/12/7334
Notification Date 06/18/2012

Improved design in CMOSF8H process for the M95256, 256 Kbit SPI bus EEPROM / industrial range

Table 1. Change Implementation Schedule

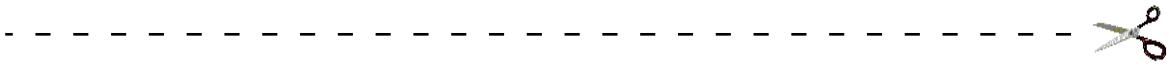
Forecasted implementation date for change	11-Jun-2012
Forecasted availabillity date of samples for customer	11-Jun-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Jun-2012
Estimated date of changed product first shipment	17-Sep-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M95256 products family
Type of change	Product design change
Reason for change	Line up to state of art of design
Description of the change	Improved design of the CMOSF8H Process Technology.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process ID is "8" for Improved F8H design
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/12/7334**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 06/18/2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Division Marketing Manager
Rodrigues, Benoit	Division Product Manager
Malbranche, Jean-Luc	Division Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

Improved design in CMOSF8H process for the M95256, 256 Kbit SPI bus EEPROM / industrial range

What is the change?

The **M95256, 256 Kbit SPI I²C bus EEPROM** product family currently produced using the CMOSF8H process technology at ST Rousset (France) 8 inch wafer diffusion plant will undergo through an **improved design** leading to die size reduction (more compact layout).
This will also allow to offer **1.7 V** – 5.5 V ("-F") Vcc range.
The M95256 with the improved design is functionally compatible to the current CMOSF8H version, as per datasheet (rev. 17 – January 2012, here attached).

Concurrent to this change, the following production rationalization will follow:

- SO8N (Narrow, 150 mils) assembled on SHD line at ST Shenzhen will use 0.8 mil Copper wire (as introduced in PCN MMS-MMY/11/6929).
- WLCSP (Wafer Level Chip scale Package): Commercial Part Number will change from M95256-RCS6TP/A to M95256-DFCS6TP/K (with smaller dimensions), PTN will be released in 2h/2012.

(See Appendix B for list of Commercial Part numbers)

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the improved design on the M95256 will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the M95256 with the improved design will ramp up from July 2012 and shipments can start from September 2012 onward (or earlier upon customer approval).

How will the change be qualified?

The M95256 with the improved design will be qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

The **Qualification Report QRMMY1125** is available and included inside this document.

What is the impact of the change?

- Form: marking change: refer to **Device marking** paragraph
- Fit: no change
- Function: no change

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: The **Mask revision** identifier is "**B**" for the CMOSF8H **improved design** version, this identifier being "A" for the current CMOSF8H version.

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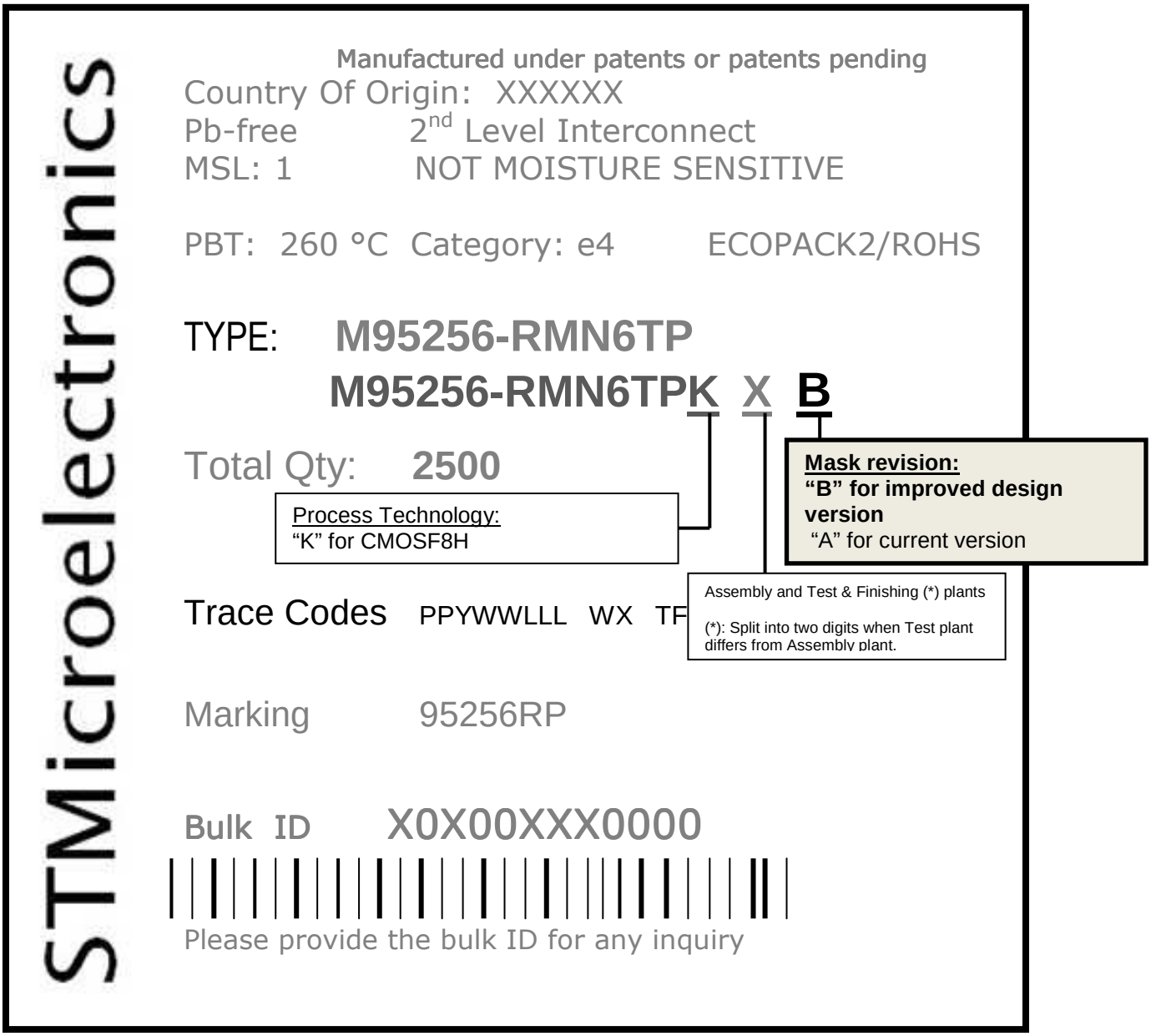
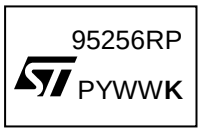
➔ *Example for M95256-RMN6TP*



How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit "T" for **Process Technology identifier** is "**8**" for the **improved design** version, this identifier being "K" for the current CMOSF8H version.

	Improved Design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
SO8N Example: M95256-BRMN6TP		

For **TSSOP8**, the difference is visible inside the product name: **improved design** version is ending by "**8**", the current version being ended by "K".
For the D version (Lockable Identification Page), the difference is visible inside the product name: improved design version is **5568D**, the current version being 556AD.

	Improved Design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
TSSOP8 Example: M95256-RDW6TP		

Legend:

P = Assembly plant
Y = Year of Assembly last digit
WW = Assembly Week
T = Process Technology code / Wafer Fab ID

For **MLP 2x3**, the difference is visible inside the product name: **improved design** version is ending by "**8**", the current version being ended by "K".

	Improved Design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
MLP 2x3 Example: M95256-RMC6TG	556**8** PYWW	556**K** PYWW

Appendix A- Product Change Information

Product family / Commercial products:	M95256 products family
Customer(s):	All
Type of change:	Product design change
Reason for the change:	Line up to state of art of design
Description of the change:	Improved design of the CMOSF8H Process Technology.
Forecast date of the change: (Notification to customer)	Week 24 / 2012
Forecast date of Qualification samples availability for customer(s):	See details in next page
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The Qualification Report **QRMMY1125** is included inside this document
Marking to identify the changed product:	Process ID is “8” for Improved F8H design
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Estimated date of first shipment:	Week 38 / 2012

Appendix B: Concerned Commercial Part Numbers:

- The following commercial part numbers will use the M95256 with the improved design:

Commercial Part Numbers	Package	Samples availability
M95256-RMN6TP (*)	SO8N	Week 29
M95256-WMN6TP	SO8N	Available
M95256-RDW6TP (*)	TSSOP8	Available
M95256-WDW6TP	TSSOP8	Week 29
M95256-RMC6TG	MLP 2x3	Week 30
M95256-RMC6TG/12	MLP 2x3	Week 32

(*) Following product line rationalization, we recommend customer to use **–R** version (**1.8 V** – 5.5 V) when –W (2.5 V – 5.5 V) is used.
For instance, **M95256-RMN6TP should be preferred** to M95256-WMN6TP.

- The following part numbers will not be kept in production, replacement part numbers are:

Current Commercial Part Numbers	Package	Replacement Commercial Part Numbers	Samples availability
M95256-D**R**DW6TP	TSSOP8	M95256-D**F**DW6TP	Week 30
M95256-**R**CS6TP/A	WLCSP	M95256-**DF**CS6TP/K	October 2012

Appendix C: Qualification Report:

See following pages

QRMMY1125
Qualification report

Improved design / M95256-R M95256-W M95256-DF using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M95256-RMN6TP M95256-WMN6TP M95256-RDW6TP M95256-WDW6TP M95256-RMC6TG M95256-RMC6TG/12 M95256-DFDW6TP M95256-DFCS6TP/K
Product description	256 Kbit serial SPI bus EEPROM with high-speed clock
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	subcon Amkor, Philippines	subcon Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	subcon Amkor, Philippines	subcon Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	subcon Amkor, Philippines	subcon Amkor, Philippines
WLCSP	subcon Stats ChipPac, Singapore	subcon Stats ChipPac, Singapore

Reliability assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the improved design M95256 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for W devices
- 1.8 to 5.5 V at –40 to 85 °C for R devices
- 1.7 to 5.5 V at –40 to 85 °C for DF devices

The CMOSF8H is a new advanced silicon process technology that is already qualified in the STMicroelectronics Rousset 8” diffusion plant, and in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24C64/M95640 and M24C32/M95320 EEPROM products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion plant.

1.2 Conclusion

The improved design M95256 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed all the reliability requirements.

Refer to *Section 3: Reliability test results* for details.

2 Device characteristics

Device description

The M95256, M95256-W, M95256-R and M95256-DF are electrically erasable programmable memory (EEPROM) devices. They are accessed by a high speed SPI-compatible bus. Their memory array is organized as 32768 × 8 bits.

The M95256-DF also offers an additional page, named the Identification Page (64 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as the Identification Page can be used to store unique identification parameters and/or parameters specific to the production line.

The device is accessed by a simple serial interface that is SPI-compatible.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95256	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)
M24256 (2)	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.
2. Die-oriented reliability tests mainly based on M24256 product (same silicon process technology, same design core between 256Kbit I2C and 256Kbit SPI / Metal mask option for bus control).

The package qualifications were mainly obtained by similarity. The product vehicles and silicon process technologies used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95M02 (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / subcon Amkor
M24M01 (2)	CMOSF8H	ST Rousset 8”	TSSOP8	ST Shenzhen / subcon Amkor
M24512	CMOSF8H	ST Rousset 8”	UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / subcon Amkor
M95M02 / M24512	CMOSF8H	ST Rousset 8”	WLCSP	subcon Stats ChipPac

1. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable to M95256.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable to M95256.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description						
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size	
						M24256	M95256
						Lot 1 (2)	Lot 2
EDR	High temperature operating life after endurance						
	AEC-Q100-005	100 000 E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	-
	Data retention after endurance						
	AEC-Q100-005	100 000 E/W cycles at 150 °C then: HTSL at 150 °C	80	1	1008 hrs	0/80	-
LTOL	Low temperature operating life						
	JESD22-A108	–40 °C, 6 V	80	1	1008 hrs	0/80	-
HTSL	High temperature storage life						
	JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80	-
WEB	Program/erase endurance cycling + bake						
	Internal spec.	1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	1 Million cycles / 48 hrs	0/80 (3)	-
ESD HBM	Electrostatic discharge (human body model)						
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	1	N/A	Pass 4000 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)						
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	1	N/A	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)						
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	1	N/A	Class II - Level A	Class II - Level A

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Die-oriented reliability tests mainly based on M24256 product (same silicon process technology, same design core between 256Kbit I2C and 256Kbit SPI / Metal mask option for bus control).
3. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95M02 (2)			M95256
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB(3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK(3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL(3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ELFR(3)	Early life failure rate								
	AEC-Q100-008	HTOL at 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Results FC W26

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable to M95256.
3. THB-, TC-, TMSK-, AC-, HTSL and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24M01 (2)			M95256
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	400	3	N/A	0/400	0/400	0/400	-
THB(3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK(3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL(3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Results FC W26

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable to M95256.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 8. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
08-Jun-2012	1	Initial release.

Document Revision History

Date	Rev.	Description of the Revision
May 02 , 2011	1.00	First draft creation

Source Documents & Reference Documents

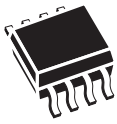
Source document Title	**Rev.:**	**Date:**

M95256-DR
M95256 M95256-W M95256-R

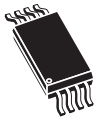
256-Kbit serial SPI bus EEPROM with high-speed clock

Features

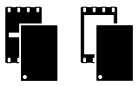
- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 256 Kbits (32 Kbytes) of EEPROM
  - Page size: 64 bytes
- Additional Write lockable Page (Identification page)
- Write (self-timed cycle)
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Write Protect: quarter, half or whole memory array
- High-speed clock frequency (20 MHz)
- Single supply voltage: 1.8 V to 5.5 V
- More than 1 million Write cycles
- More than 40-year data retention
- Enhanced ESD Protection
- Packages
  - ECOPACK2® (RoHS compliant and Halogen-free)



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width



UFDFPN8 (MB, MC)
2 × 3 mm (MLP)

WLCSP (CS)

Contents

List of tables

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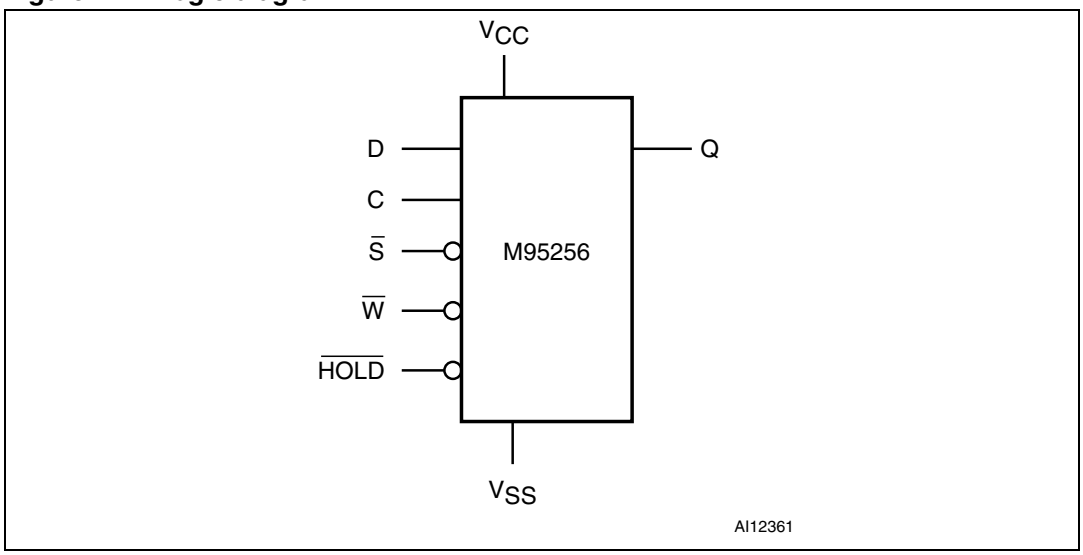
1 Description

The M95256, M95256-W, M95256-R and M95256-DR are electrically erasable programmable memory (EEPROM) devices. They are accessed by a high speed SPI-compatible bus. Their memory array is organized as 32768 × 8 bits.

The M95256-DR also offers an additional page, named the Identification Page (64 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as the Identification Page can be used to store unique identification parameters and/or parameters specific to the production line.

The device is accessed by a simple serial interface that is SPI-compatible.

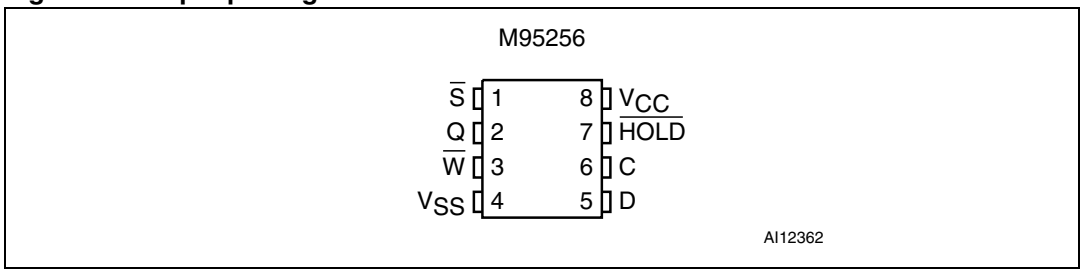
Figure 1. Logic diagram



The bus signals are C, D and Q, as shown in *Table 1* and *Figure 1*.

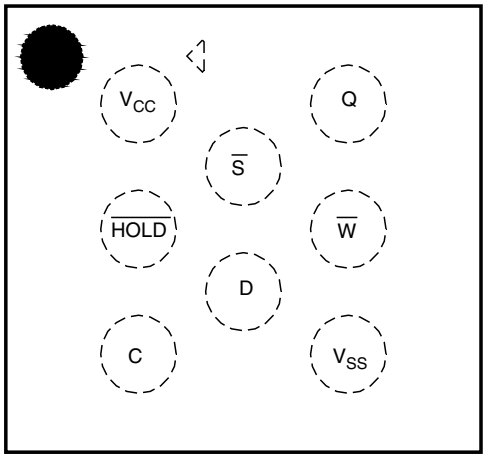
The device is selected when Chip Select ($\overline{S}$) is taken low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

Figure 2. 8-pin package connections



1. See *Section 10: Package mechanical data* for package dimensions, and how to identify pin-1.

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)



Caution: As EEPROM cells loose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

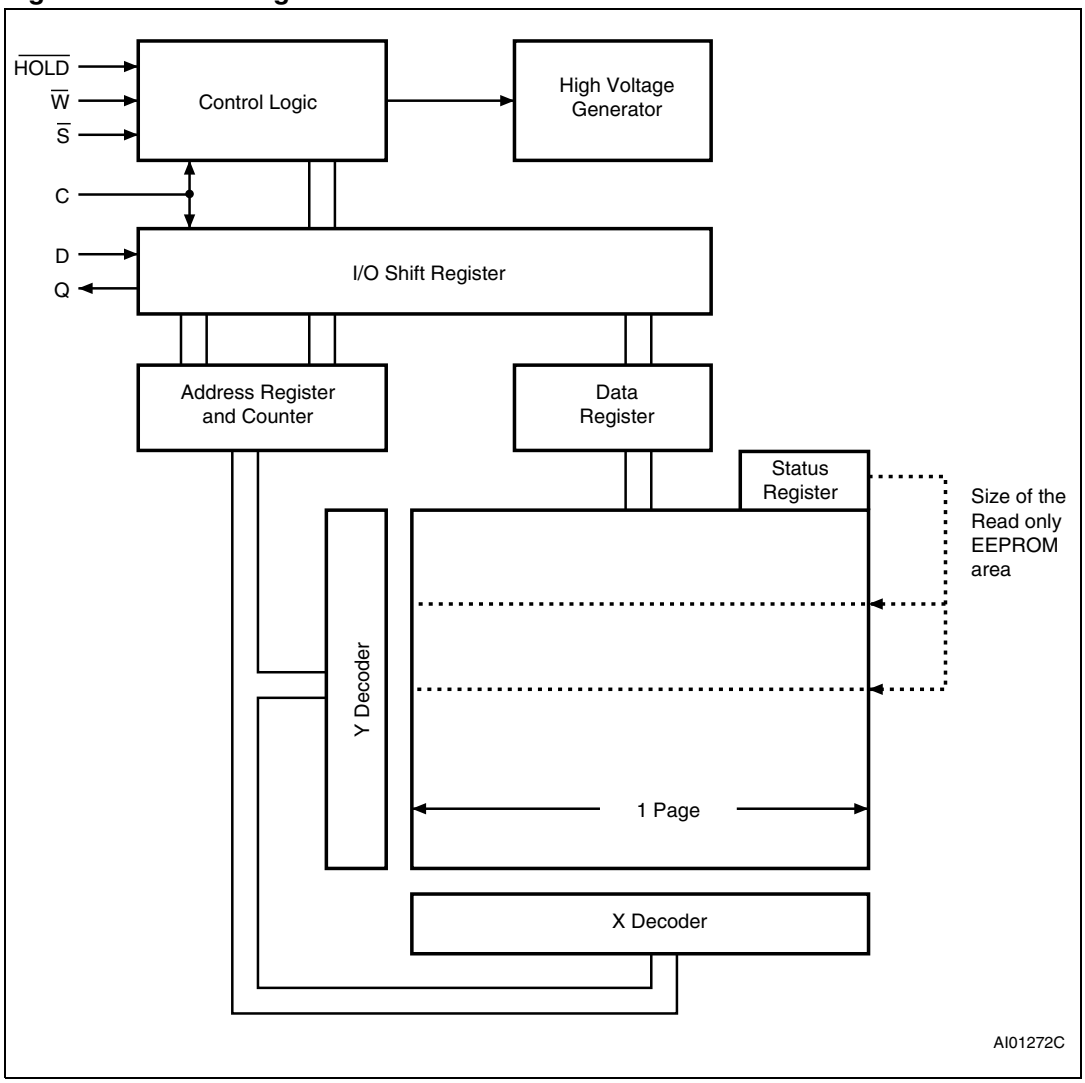
Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

2 Memory organization

The memory is organized as shown in *Figure 4*.

Figure 4. Block diagram



3 Signal description

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

3.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

3.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

3.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data output (Q) changes after the falling edge of Serial Clock (C).

3.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device is in Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

3.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

3.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all write instructions.

3.7 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3.8 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC(min)}$, $V_{CC(max)}$] range must be applied (see *Table 8*, *Table 9*, *Table 10*).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

3.8.1 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal Reset threshold voltage (this threshold is defined in DC tables as V_{RES}). (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8*, *Table 9*, *Table 10*).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in Standby Power mode,
- deselected (note that a further instruction must be preceded by a falling edge on Chip Select ($\overline{S}$) to be executed),
- Status Register value:
  - the Write Enable Latch (WEL) is reset to 0,
  - Write In Progress (WIP) is reset to 0,
  - The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits)

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. However, the device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [$V_{CC(min)}$, $V_{CC(max)}$] range, as defined in *Table 8*, *Table 9*, *Table 10*.

3.8.2 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage, it is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 17*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been High, prior to going Low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 8*, *Table 9*, *Table 10* and the rise time must not vary faster than 1 V/µs.

3.8.3 Power-down

During Power-down (continuous decrease of V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 8*, *Table 9*, *Table 10*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- in Standby Power mode (there should not be an internal Write cycle in progress).

4 Operating features

4.1 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

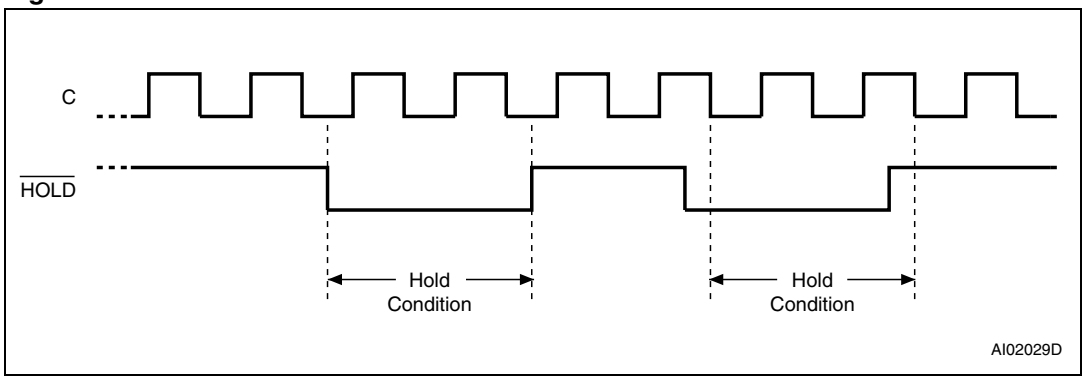
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven low at the same time as Serial Clock (C) already being low (as shown in *Figure 5*).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven high at the same time as Serial Clock (C) already being low.

Figure 5 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

Figure 5. Hold condition activation



4.2 Status Register

Figure 4 shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. For a detailed description of the Status Register bits, see *Section 5.3: Read Status Register (RDSR)*.

4.3 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked to ensure that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{W}$) signal is used to protect the Block Protect (BP1, BP0) bits of the Status Register.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C):

- The ‘last bit of the instruction’ can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The ‘next rising edge of Serial Clock (C)’ might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 2. Write-protected block size

Status Register bits		Protected block	Protected array address
BP1	BP0		M95256, M95256-W, M95256-R
0	0	none	none
0	1	Upper quarter	6000h - 7FFFh
1	0	Upper half	4000h - 7FFFh
1	1	Whole memory	0000h - 7FFFh

5 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in *Table 3*), the device is automatically deselected.

Table 3. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

Table 4. M95256-D instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010
Read Identification Page	Reads the page dedicated to identification.	1000 0011(1)
Write Identification Page	Writes the page dedicated to identification.	1000 0010(1)
Read Lock Status	Reads the lock status of the Identification Page.	1000 0011(2)
Lock ID	Locks the Identification page in read-only mode.	1000 0010(2)

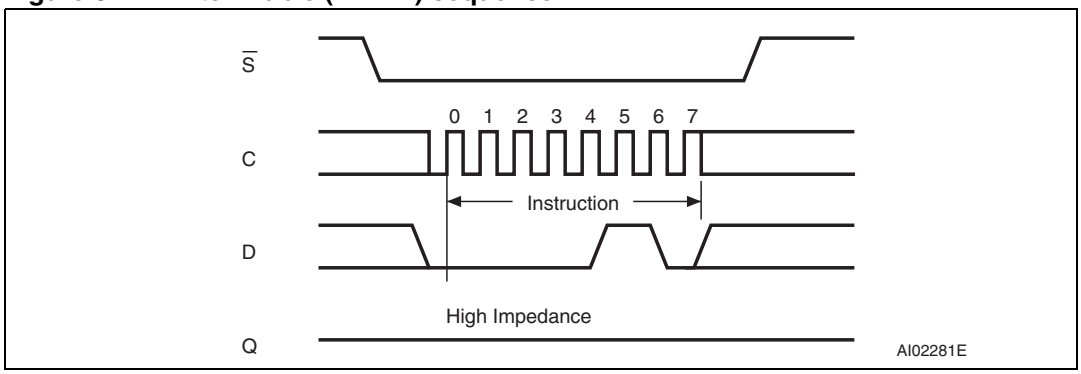
1. Address bit A10 must be 0, all other address bits are Don't Care (see *5.7* and *5.8* for more details).
2. Address bit A10 must be 1, all other address bits are Don't Care (see *5.9* and *5.10* for more details).

5.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 6*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 6. Write Enable (WREN) sequence



5.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

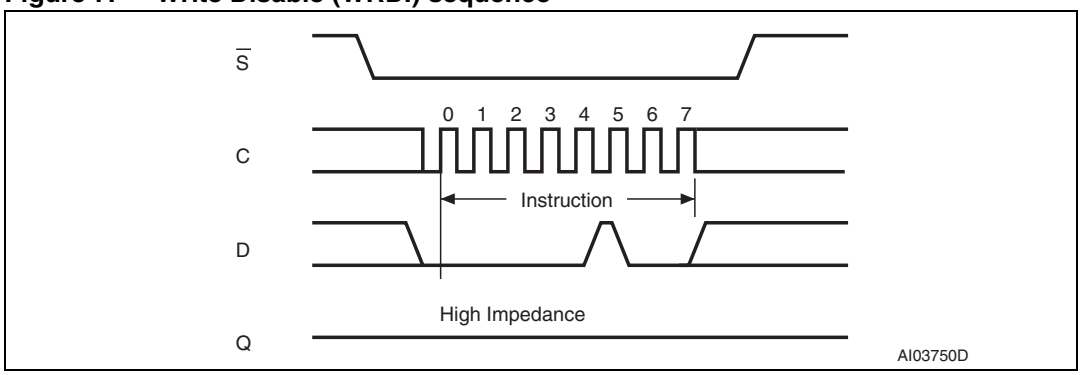
As shown in *Figure 7*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion

Figure 7. Write Disable (WRDI) sequence



5.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 8*.

The status and control bits of the Status Register are as follows:

5.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress. When reset to 0, no such cycle is in progress.

5.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

5.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is/are set to 1, the relevant memory area (as defined in *Table 5*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

5.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 5. Status Register format

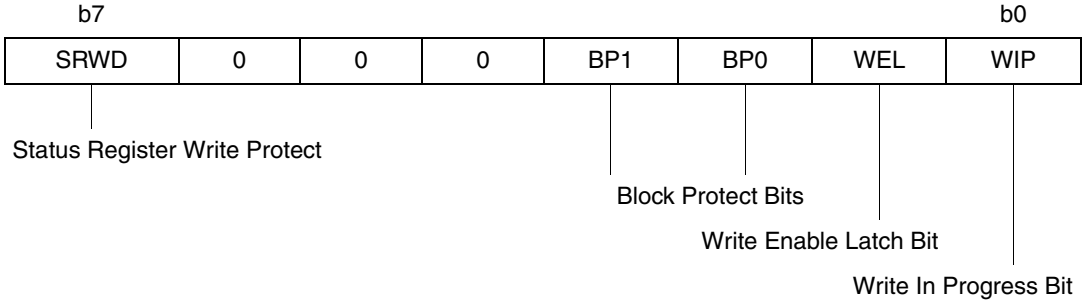
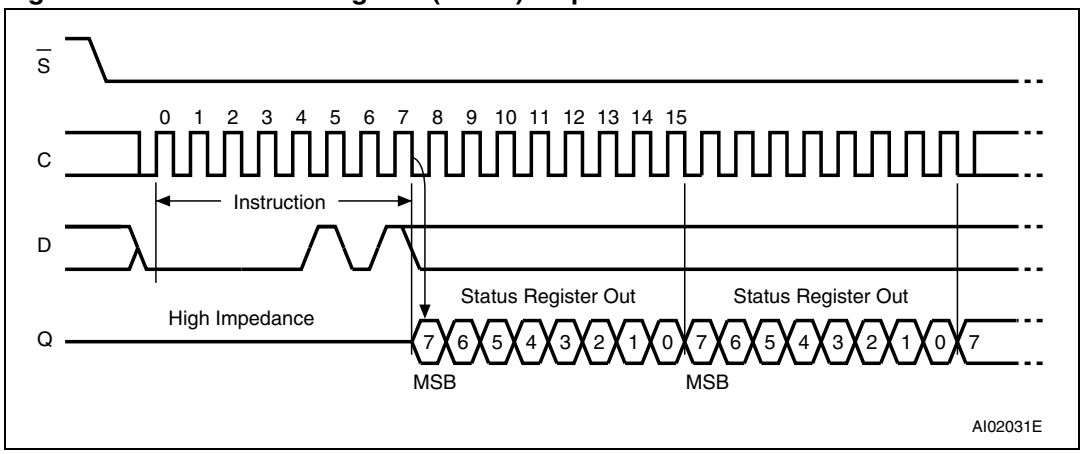


Figure 8. Read Status Register (RDSR) sequence



5.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, the data byte on Serial Data Input (D) and the Chip Select ($\overline{S}$) driven High. Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not properly executed.

The instruction sequence is shown in *Figure 9*.

Driving the Select ($\overline{S}$) High at a byte boundary of the input data triggers the self timed Write cycle, and continues for a period t_W (as specified in *Table 17*, *Table 18*, *Table 19* and *Table 20*). While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit: the WIP bit is 1 during the self-timed Write cycle t_W, and is 0 when the Write cycle is completed. The WEL bit (Write Enable Latch) is also reset when the Write cycle t_W is completed.

The Write Status Register (WRSR) instruction allows the user to change the values of the BP1, BP0 bits and the SRWD bit:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read only, as defined in *Table 2*.
- The SRWD bit (Status Register Write Disable bit), in accordance with the signal read on the Write Protect pin ($\overline{W}$), allows the user to set or reset the Write protection mode of the Status Register itself, as defined in *Table 6*. When in Write Protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W Write cycle.

The Write Status Register (WRSR) instruction has no effect on bits b6, b5, b4, b1, b0 of the Status Register. Bits b6, b5, b4 are always read as 0.

Table 6. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write-protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Write-protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *Table 6*.

The protection features of the device are summarized in *Table 6*.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the Write Protect ($\overline{W}$) input pin.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$) input pin:

- If Write Protect ($\overline{W}$) input pin is driven high, it is possible to write to the Status Register, provided that the WEL bit has previously been set by a WREN instruction.
- If Write Protect ($\overline{W}$) input pin is driven low, it is not possible to write to the Status Register even if the WEL bit has been previously set by a WREN instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

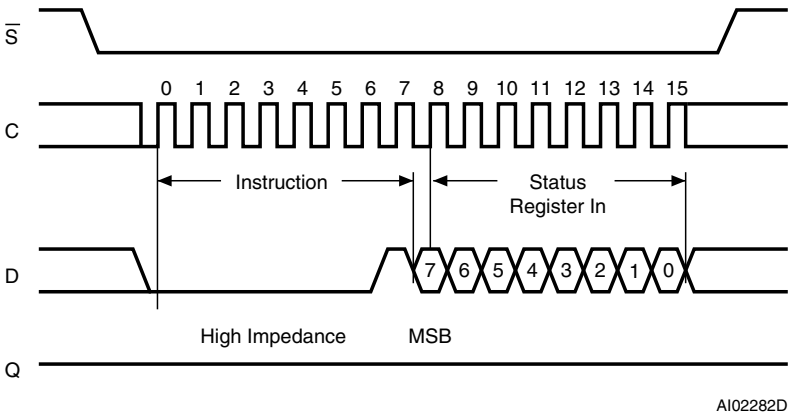
Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- either by setting the SRWD bit after driving Write Protect ($\overline{W}$) input pin low,
- or by driving Write Protect ($\overline{W}$) input pin low after setting the SRWD bit.

Once entered in the Hardware Protected mode (HPM), the only way to exit the HPM mode is to pull high the Write Protect ($\overline{W}$) input pin.

If Write Protect ($\overline{W}$) input pin is permanently tied high, the Hardware Protected mode (HPM) can never be activated, and only the Software Protected mode (SPM), using the Block Protect (BP1, BP0) bits of the Status Register, can be used.

Figure 9. Write Status Register (WRSR) sequence



5.5 Read from Memory Array (READ)

As shown in *Figure 10*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

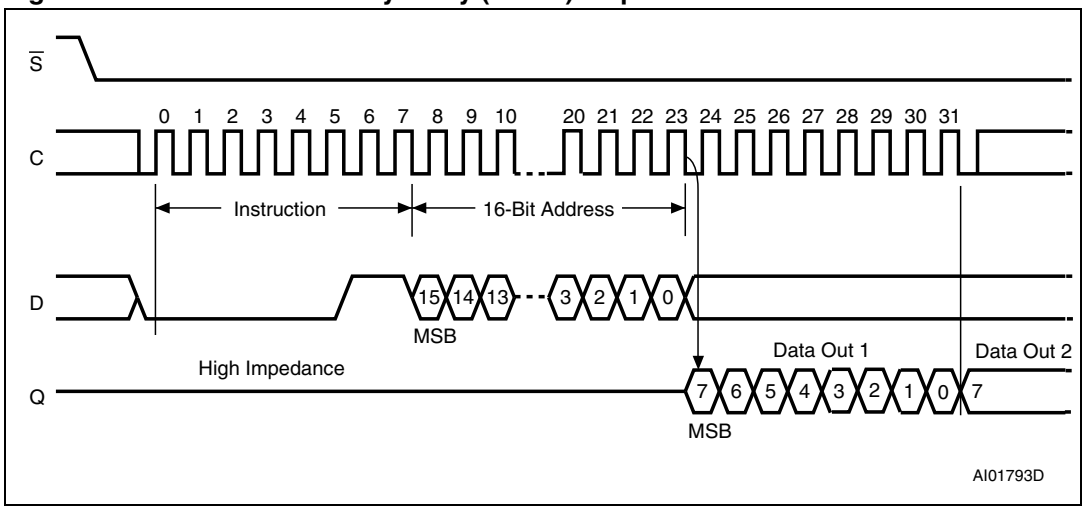
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 10. Read from Memory Array (READ) sequence



1. The most significant address bit (b15) is Don't Care.

5.6 Write to Memory Array (WRITE)

As shown in *Figure 11*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address bytes, and at least one data byte are then shifted in, on Serial Data input (D). The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the rising edge of Chip Select ($\overline{S}$), continues for a period t_{WC} (as specified in *Table 17*, *Table 18*, *Table 19* and *Table 20*), at the end of which the Write in Progress (WIP) bit is reset to 0.

In the case of *Figure 11*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 12*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

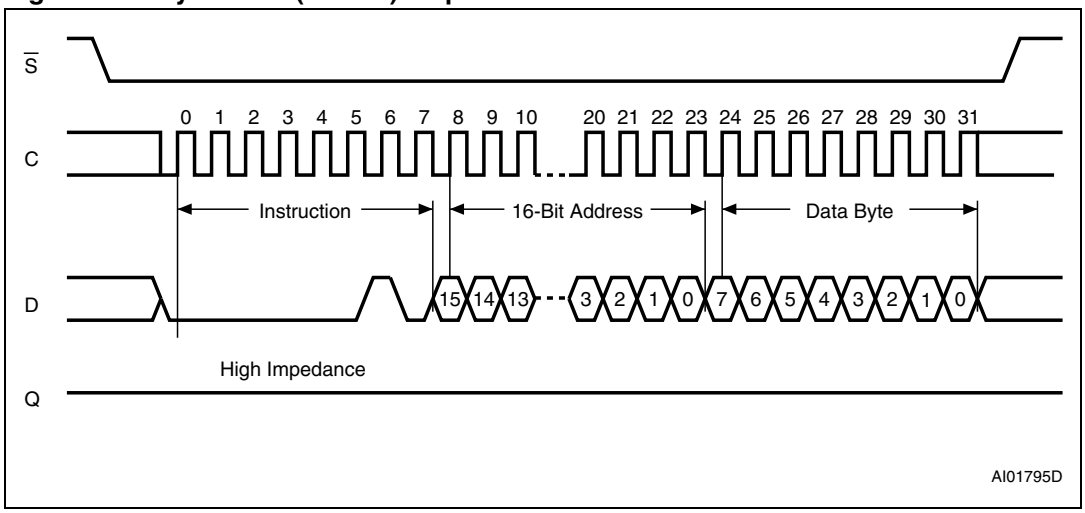
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there is overwritten with the incoming data. (The page size of these devices is 64 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

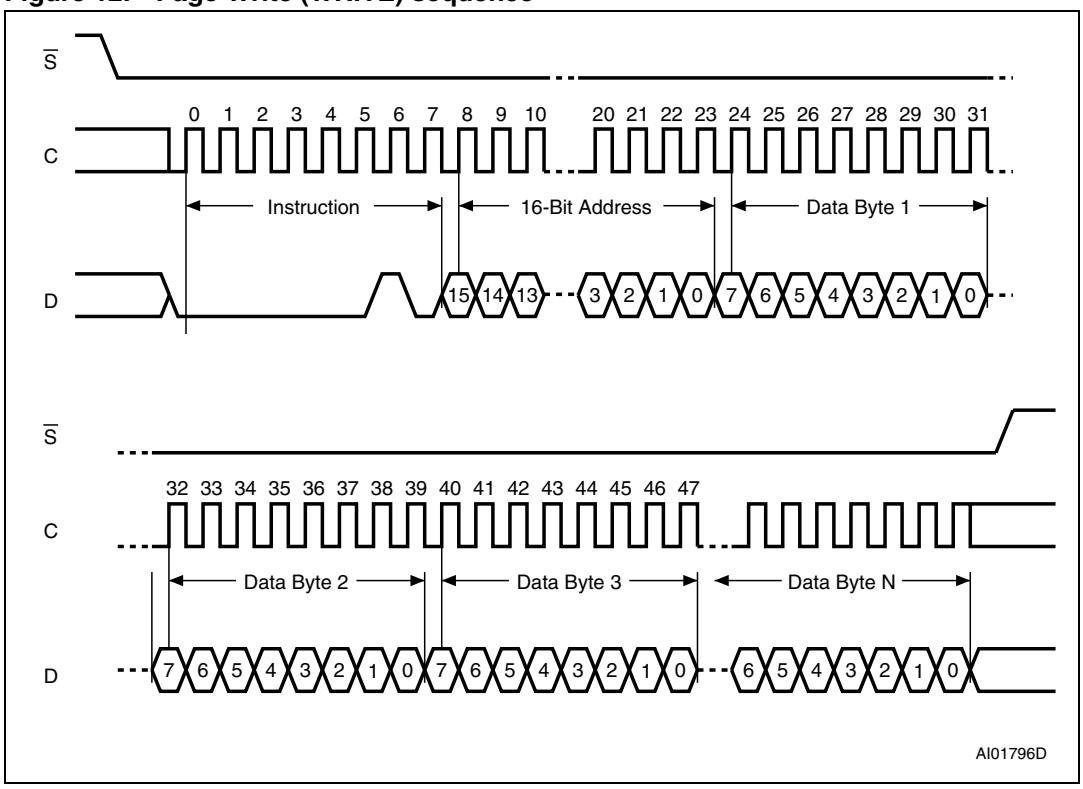
Note: The self-timed Write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 11. Byte Write (WRITE) sequence



1. The most significant address bit (b15) is Don't Care.

Figure 12. Page Write (WRITE) sequence



1. The most significant address bit (b15) is Don't Care.

5.6.1 ECC (Error Correction Code) and Write cycling

The M95256 and M95256-D devices offer an ECC (Error Correction Code) logic which compares each 4-byte word with its associated 6 EEPROM bits of ECC. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a Read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

If a single byte has to be written, 4 bytes are internally modified (plus the ECC bits). That is, the addressed byte is cycled together with the three other bytes making up the word. It is therefore recommended to write data word by word (4 bytes) at address 4*N (where N is an integer) in order to benefit from the larger amount of Write cycles.

The M95256 and M95256-D devices are qualified at 1 million (1 000 000) Write cycles, using a cycling routine that writes to the device in multiples of 4-byte words.

5.7 Read Identification Page (available only in M95256-DR devices)

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

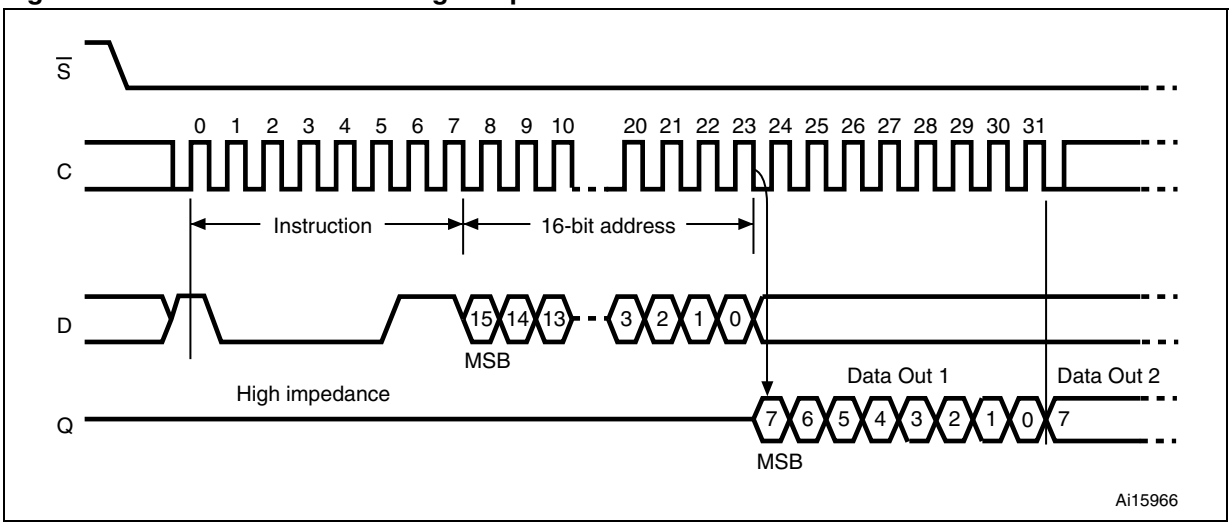
Reading this page is achieved with the Read Identification Page instruction (see *Table 4*). The Chip Select signal (S) is first driven low, the bits of the instruction byte and address bytes are then shifted in, on Serial Data input (D). Address bit A10 must be 0, address bits [A15:A11] and [A9:A6] are Don't Care, and the data byte pointed to by [A5:A0] is shifted out on Serial Data output (Q). If Chip Select (S) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

The number of bytes to read in the ID page must not exceed the page boundary, otherwise unexpected data is read (e.g. when reading the ID page from location 24d, the number of bytes should be less than or equal to 40d, as the ID page boundary is 64 bytes).

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle. The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 13. Read Identification Page sequence

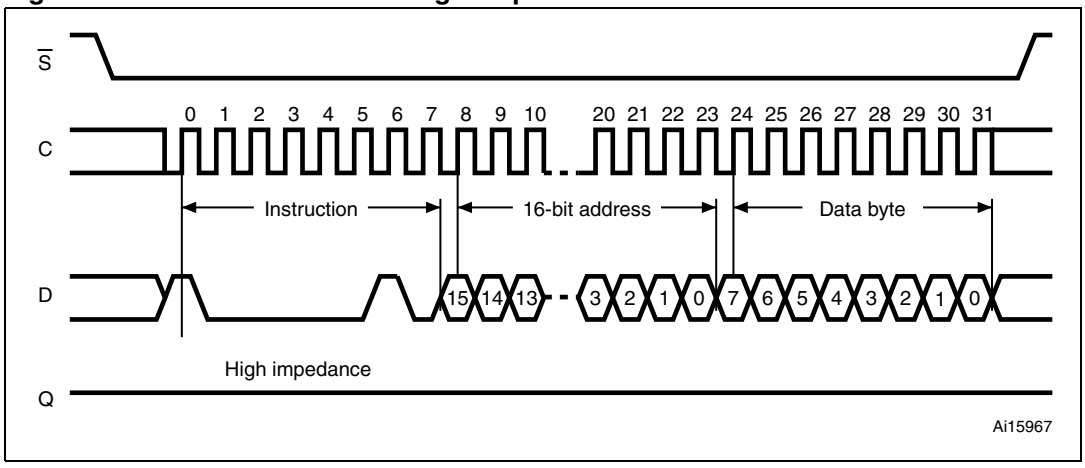


5.8 Write Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

Writing this page is achieved with the Write Identification Page instruction (see *Table 4*). The Chip Select signal (S) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in on Serial Data input (D). Address bit A10 must be 0, address bits [A15:A11] and [A9:A6] are Don't Care, the [A5:A0] address bits define the byte address inside the identification page. The instruction sequence is shown in *Figure 14*.

Figure 14. Write Identification Page sequence

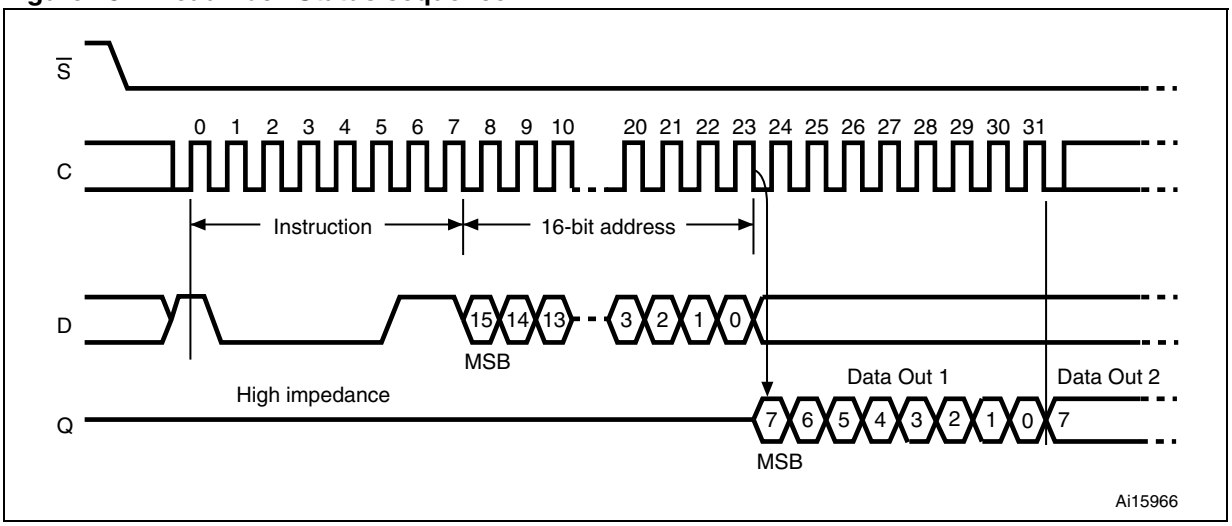


5.9 Read Lock Status (available only in M95256-DR devices)

The Read Lock Status instruction (see *Table 4*) allows to check if the Identification Page is locked (or not) in read-only mode. The Read Lock Status sequence is defined with the Chip Select (S) first driven low. The bits of the instruction byte and address bytes are then shifted in on Serial Data input (D). Address bit A10 must be 1, all other address bits are Don't Care. The Lock bit is the LSB (least significant bit) of the byte read on Serial Data output (Q). It is set to 1 when the lock is active and set to 0 when the lock is not active. If Chip Select ($\overline{S}$) continues to be driven low, the same data byte is shifted out. The read cycle is terminated by driving Chip Select ($\overline{S}$) high.

The instruction sequence is shown in *Figure 15*.

Figure 15. Read Lock Status sequence



5.10 Lock ID (available only in M95256-DR devices)

The Lock ID instruction permanently locks the Identification Page in read-only mode. Before this instruction can be accepted, a Write Enable (WREN) instruction must have been executed. The Lock ID instruction is issued by driving Chip Select ($\overline{S}$) low, sending the instruction code, the address and a data byte on Serial Data input (D), and driving Chip Select ($\overline{S}$) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

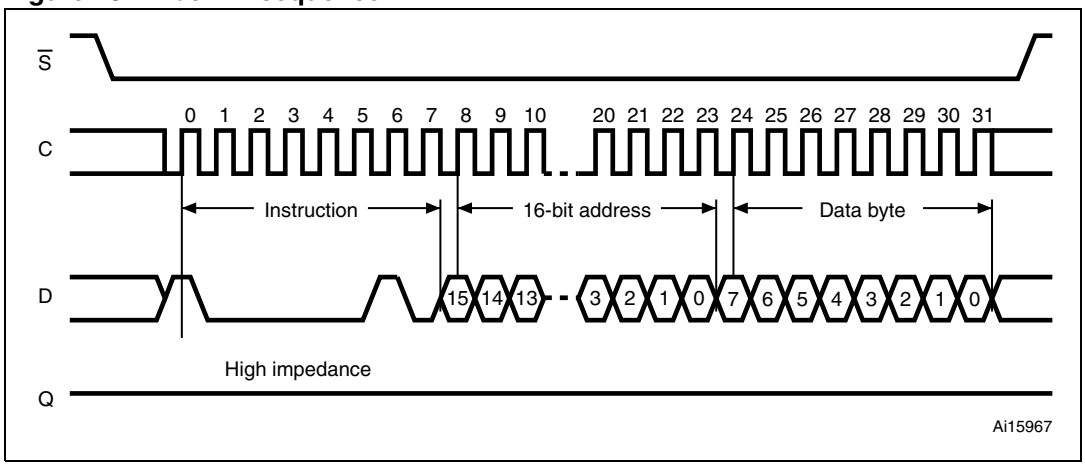
Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Lock ID instruction is not executed.

Driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is t_W (as specified in *Table 20*). The instruction sequence is shown in *Figure 16*.

The instruction is not accepted, and so not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by previously executing a Write Enable instruction)
- if Status register bits (BP1,BP0) = (1,1)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that was latched in)
- if the Identification page is locked by the Lock Status bit

Figure 16. Lock ID sequence



6 Delivery state

The device is delivered with all the memory array cells set to 1 (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

7 Connecting to the SPI bus

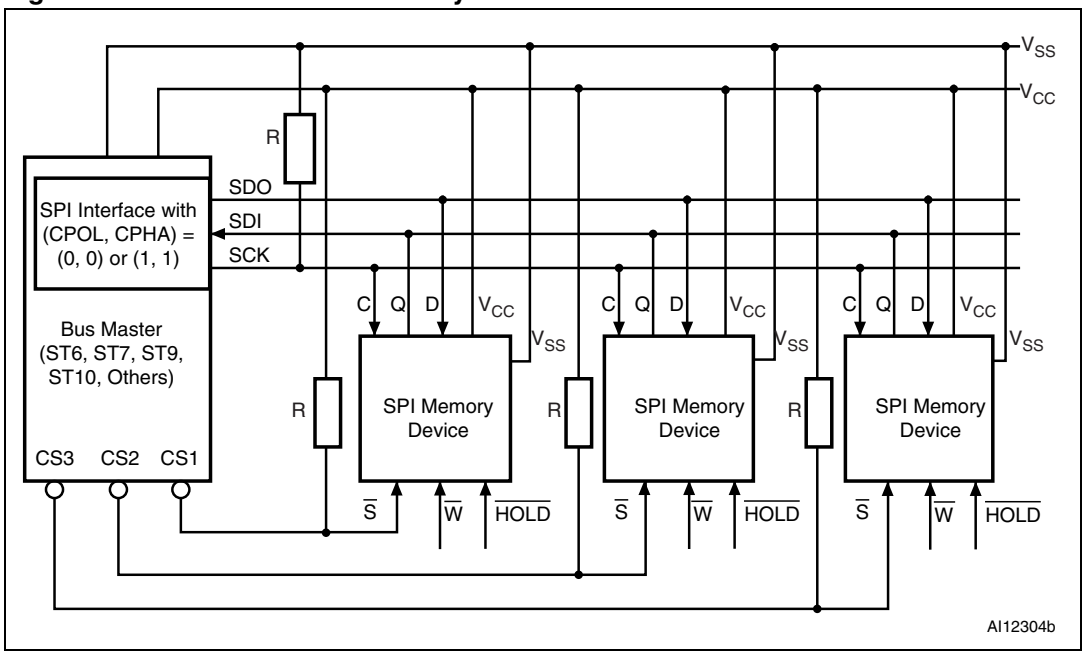
These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted into the device, the most significant bit first. The Serial Data input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, the most significant bit first. The Serial Data output (Q) is latched on the first falling edge of the Serial Clock (C) after the instructions (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 17 shows an example of three memory devices connected to an MCU, on an SPI bus. Only one memory device is selected at a time, so only one memory device drives the Serial Data output (Q) line at a time; the other memory devices are high impedance.

Figure 17. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

A pull-up resistor connected on each /S input (represented in *Figure 7*) ensures that each slave device on the SPI bus is not selected if the bus master leaves the /S line in the high impedance state.

In applications where the bus master might enter a state where all SPI bus inputs/outputs would be in high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor. Thus, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high). This ensures that $\overline{S}$ and C do not become high at the same time, and that the t_{SHCH} requirement is met. R typical value is 100 kΩ

7.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

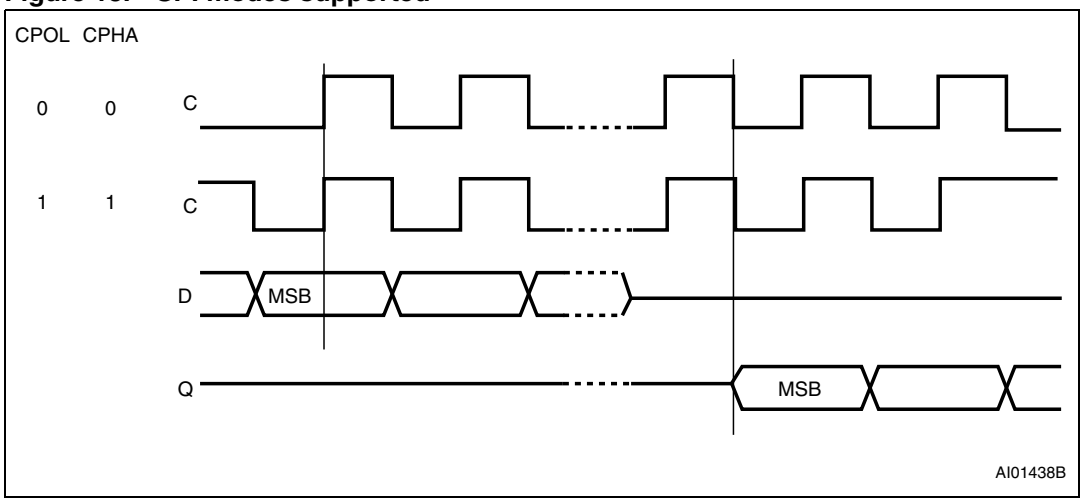
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 18*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 18. SPI modes supported



8 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these conditions, or at any other condition outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient temperature with power applied	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	–5	-	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)		4000(3)	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100pF, R1=1500 Ω, R2=500 Ω)
3. V_{ESD} is 3000 V (max) for the M95256 identified with process letter K.

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M95256)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature (device grade 3)	–40	125	°C

Table 9. Operating conditions (M95256-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 10. Operating conditions (M95256-R and M95256-DR)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 11. AC measurement conditions(1)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30 or 100(2)		pF
t_r, t_f	Input rise and fall times		25	ns
$V_{hi\text{-}lo}$	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
$V_{ref(t)}$	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.
2. 100 pF when the clock frequency f_C is less than 10 MHz, 30 pF when the clock frequency f_C is equal to or greater than 10 MHz.

Figure 19. AC measurement I/O waveform

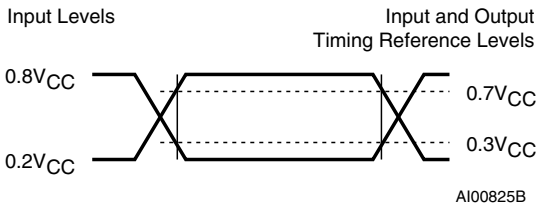


Table 12. Capacitance(1)

Symbol	Parameter	Test condition	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V	8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V	8	pF
	Input capacitance (other pins)	V_{IN} = 0 V	6	pF

1. Sampled only, not 100% tested.

Table 13. Memory cell characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
N_{cycle}	Endurance	T_A = 25°C, 1.8V < V_{cc} < 5.5V	1,000,000	-	Write cycle

Note: This parameter is not tested but established by characterization and qualification. To estimate endurance in a specific application, please refer to AN2014.

Table 14. DC characteristics (M95256, device grade 3)

Symbol	Parameter	Test conditions specified in *Table 7* and *Table 11*	Min.	Max.	Unit
I_{LI}	Input leakage current	V_{IN} = V_{SS} or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 5 V, Q = open		4	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S}$ = V_{CC}, V_{CC} = 5 V, V_{IN} = V_{SS} or V_{CC}		5	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}(1)	Output low voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH}(1)	Output high voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 15. DC characteristics (M95256-W, device grade 6)

Symbol	Parameter	Test conditions specified in *Table 9* (grade 6) and *Table 11*	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC}= 2.5 V, C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, Q = open		3	mA
		V_{CC}= 2.5 V, C = 0.1V_{CC}/0.9V_{CC} at 10 MHz, Q = open		4(1)	mA
		V_{CC}= 5.5 V, C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, Q = open		5	mA
		V_{CC}= 5.5 V, C = 0.1V_{CC}/0.9V_{CC} at 20 MHz, Q = open		5(2)	mA
I_{CC0}(3)	Supply current (Write)	During t_W, $\overline{S} = V_{CC}$, 2.5 V < V_{CC} < 5.5 V		5	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}$, V_{CC} = 5.5 V, $V_{IN} = V_{SS}$ or V_{CC},		5(4)	µA
		$\overline{S} = V_{CC}$, V_{CC} = 2.5 V, $V_{IN} = V_{SS}$ or V_{CC},		5(5)	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V and I_{OL} = 1.5 mA or V_{CC} = 5 V and I_{OL} = 2 mA		0.4	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V and I_{OH} = –0.4 mA or V_{CC} = 5 V and I_{OH} = –2 mA	0.8 V_{CC}		V

1. 2 mA for the M95256 devices identified with process letter K
2. For the M95256 devices identified with process letter K
3. Characterized value, not tested in production
4. 3 µA for the M95256 devices identified with process letter K
5. 2 µA for the M95256 devices identified with process letter K.

Table 16. DC characteristics (M95256-W, device grade 3)

Symbol	Parameter	Test conditions specified in *Table 9* (grade 3) and *Table 11*	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		3	mA
I_{CC0}(1)	Supply current (Write)	During t_W, $\overline{S} = V_{CC}$, 2.5 V < V_{CC} < 5.5 V		6	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} 2.5 V < V_{CC} < 5.5 V		5	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V

1. Characterized value, not tested in production.

Table 17. DC characteristics (M95256-R, M95256-DR, device grade 6)

Symbol	Parameter	Test conditions specified in *Table 10* and *Table 11* (1)	Min	Max	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, C = 0.1V_{CC}/0.9V_{CC} at 2 MHz, Q = open		1 (2)	mA
		V_{CC} = 1.8 V, C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, Q = open		2(3)	
I_{CC0} (4)	Supply current (Write)	V_{CC} = 1.8 V, during t_W, $\overline{S} = V_{CC}$		3	mA
I_{CC1}	Supply current (Standby Power mode)	V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		3(5)	µA
V_{IL}	Input low voltage	1.8 V ≤V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage	1.8 V ≤V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
V_{OH}	Output high voltage	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V

1. If the application uses the M95256-R, M95256-DR device with 2.5 V < VCC < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 15: DC characteristics (M95256-W, device grade 6)* instead of the above table.
2. 2 mA for the M95256 devices identified with process letter K
3. Only the M95256 devices identified with process letter K
4. Characterized value, not tested in production
5. 1 µA for the M95256 devices identified with process letter K.

Table 18. AC characteristics (M95256, device grade 3)

Test conditions specified in *Table 8* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH} (1)	t_{CLH}	Clock high time	90		ns
t_{CL} (1)	t_{CLL}	Clock low time	90		ns
t_{CLCH} (2)	t_{RC}	Clock rise time		1	µs
t_{CHCL} (2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ} (2)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH} (2)	t_{RO}	Output rise time		50	ns
t_{QHQL} (2)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$
2. Value guaranteed by characterization, not tested in production.

Table 19. AC characteristics, M95256-W, device grade 6

Test conditions specified in *Table 9* (grade 6) and *Table 11*			Current and new products C_L = 100 pF		New products (1) C_L = 30 pF				Unit
					$V_{cc} \geq 2.5V$		$V_{cc} \geq 4.5V$		
Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	
f_C	f_{SCK}	Clock frequency	D.C.	5	D.C.	10	D.C.	20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		30		15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		30		15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		40		20		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		30		15		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		30		15		ns
t_{CH} (2)	t_{CLH}	Clock high time	90		40		20		ns
t_{CL} (2)	t_{CLL}	Clock low time	90		40		20		ns
t_{CLCH} (2)	t_{RC}	Clock rise time		1		2		2	µs
t_{CHCL} (2)	t_{FC}	Clock fall time		1		2		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		10		5		ns
t_{CHDX}	t_{DH}	Data in hold time	30		10		10		ns
t_{HHCH}		Clock low hold time after HOLD not active	70		30		15		ns
t_{HLCH}		Clock low hold time after HOLD active	40		30		15		ns
t_{CLHL}		Clock low setup time before HOLD active	0		0		0		ns
t_{CLHH}		Clock low setup time before HOLD not active	0		0		0		ns
t_{SHQZ} (3)	t_{DIS}	Output disable time		100		40		20	ns
t_{CLQV}	t_V	Clock low to output valid		60		40		20	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		0		ns
t_{QLQH} (3)	t_{RO}	Output rise time		50		20		10	ns
t_{QHQL} (3)	t_{FO}	Output fall time		50		20		10	ns
t_{HHQV}	t_{LZ}	HOLD high to output valid		50		40		20	ns
t_{HLQZ} (3)	t_{HZ}	HOLD low to output High-Z		100		40		20	ns
t_W	t_{WC}	Write time		5		5		5	ms

1. New products are M95256 devices identified with process letter K
2. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$
3. Value guaranteed by characterization, not tested in production.

Table 20. AC characteristics (M95256-W, device grade 3)

Test conditions specified in *Table 9* (grade 6) and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH} (1)	t_{CLH}	Clock high time	90		ns
t_{CL} (1)	t_{CLL}	Clock low time	90		ns
t_{CLCH} (2)	t_{RC}	Clock rise time		1	µs
t_{CHCL} (2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ} (2)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH} (2)	t_{RO}	Output rise time		50	ns
t_{QHQL} (2)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$
2. Value guaranteed by characterization, not tested in production.

Table 21. AC characteristics (M95256-DR, M95256-R device grade 6)

Test conditions specified in *Table 10* and *Table 11*											
Symbol	Alt.	Parameter	Current products (1)		New products (2)						Unit
					$V_{CC} \geq 1.8V$		$V_{CC} \geq 2.5V$		$V_{CC} \geq 4.5V$		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_C	f_{SCK}	Clock frequency		2		5		10		20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	200		60		30		15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	200		60		30		15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	200		90		40		20		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	200		60		30		15		ns
t_{CHSL}		$\overline{S}$ not active hold time	200		60		30		15		ns
t_{CH} (3)	t_{CLH}	Clock high time	200		80		40		20		ns
t_{CL} (3)	t_{CLL}	Clock low time	200		80		40		20		ns
t_{CLCH} (4)	t_{RC}	Clock rise time		1		2		2		2	µs
t_{CHCL} (4)	t_{FC}	Clock fall time		1		2		2		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	40		20		10		5		ns
t_{CHDX}	t_{DH}	Data in hold time	50		20		10		10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	140		60		30		15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	90		60		30		15		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		0		0		0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		0		0		0		ns
t_{SHQZ} (4)	t_{DIS}	Output disable time		250		80		40		20	ns
t_{CLQV}	t_V	Clock low to output valid		150		80		40		20	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		0		0		ns
t_{QLQH} (4)	t_{RO}	Output rise time		100		20		20		10	ns
t_{QHQL} (4)	t_{FO}	Output fall time		100		20		20		10	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		100		80		40		20	ns
t_{HLQZ} (4)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		250		80		40		20	ns
t_W	t_{WC}	Write time		5		5		5		5	ms

1. Current products are identified by process letters “AB”.
2. New products are the M95256 devices identified with the process letter K.
3. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$.
4. Value guaranteed by characterization, not 100% tested in production.

Figure 20. Serial input timing

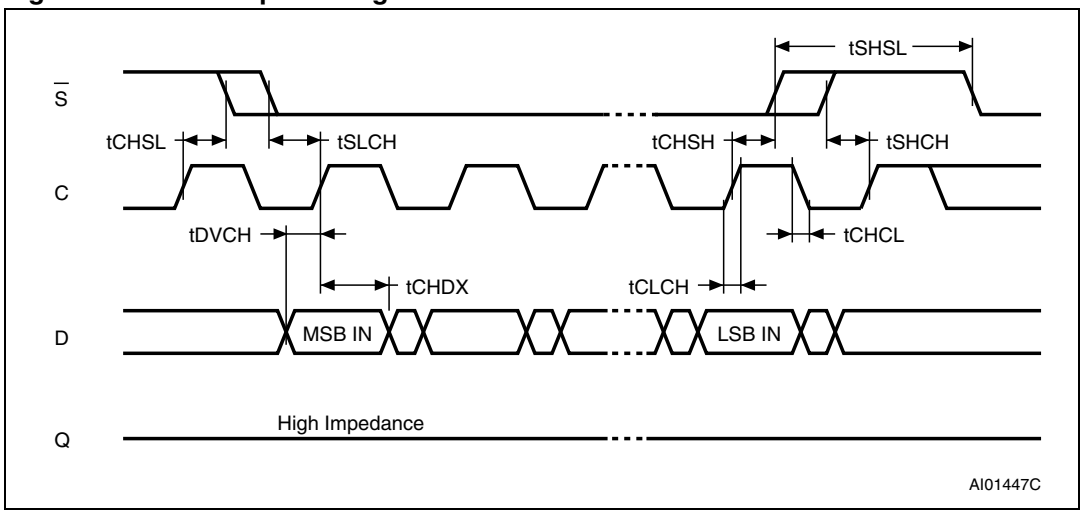


Figure 21. Hold timing

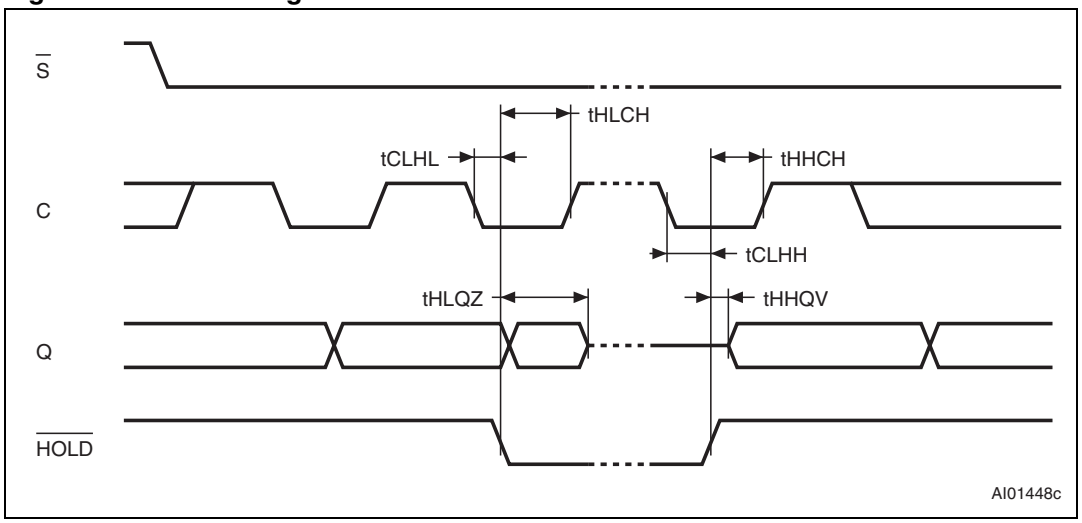
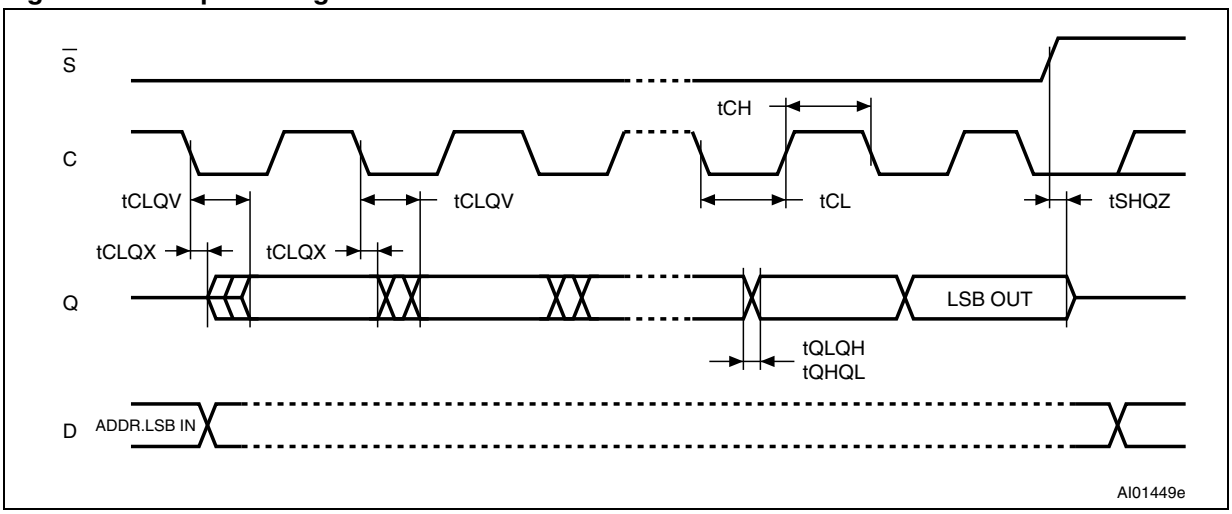


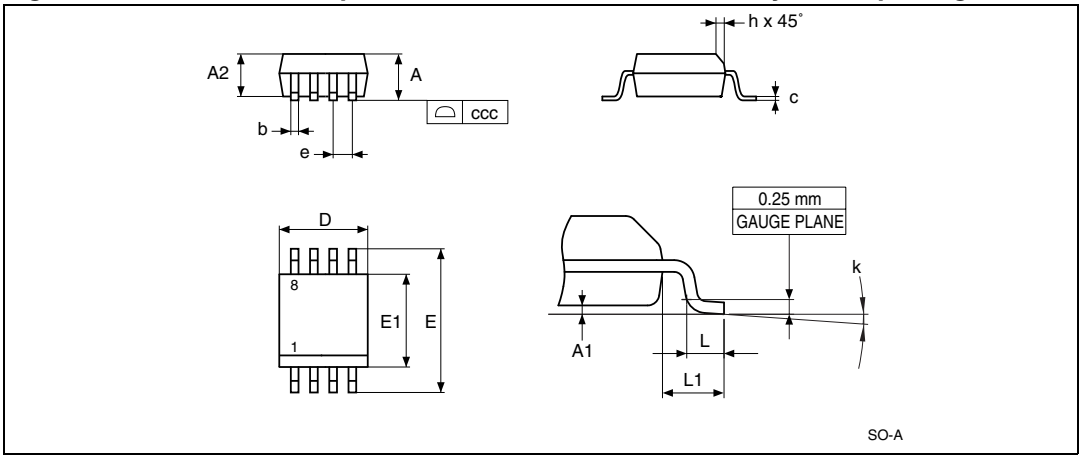
Figure 22. Output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers the M95256 in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 23. SO8N – 8 lead plastic small outline, 150 mils body width, package outline



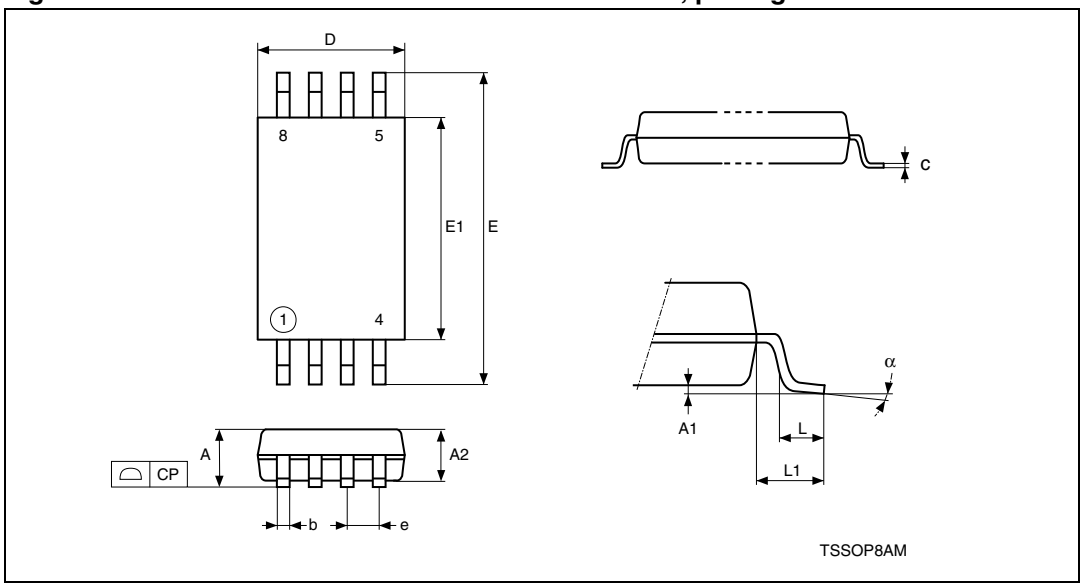
1. Drawing is not to scale.

Table 22. SO8N – 8 lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches (1)		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270			0.0500		
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 24. TSSOP8 – 8 lead thin shrink small outline, package outline



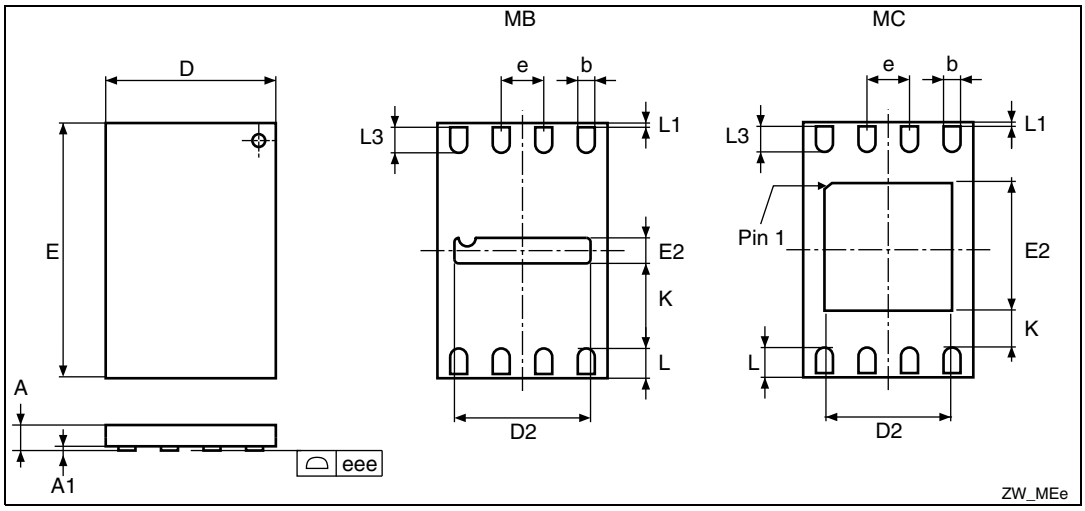
1. Drawing is not to scale.

Table 23. TSSOP8 – 8 lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches [1]		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650			0.0256		
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 25. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline



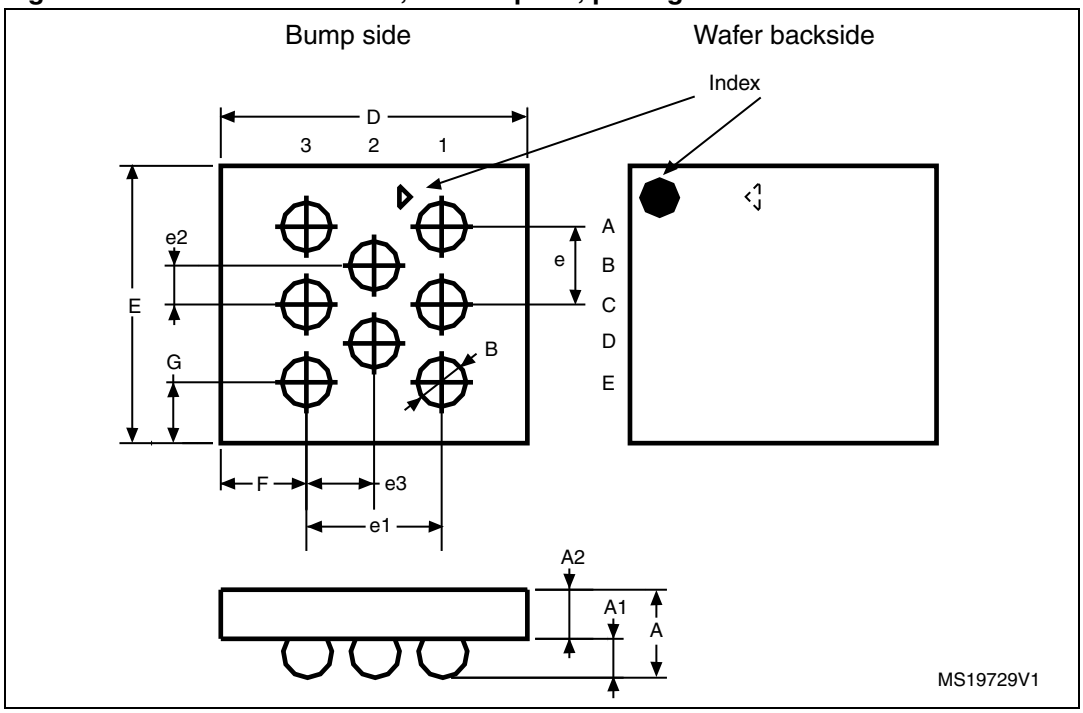
1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 24. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches (1)		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MB)	1.600	1.500	1.700	0.0630	0.0591	0.0669
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MB)	0.200	0.100	0.300	0.0079	0.0039	0.0118
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MB)		0.800			0.0315	
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee (2)		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 26. M95256-DR WLCSP, 0.5 mm pitch, package outline



1. Drawing is not to scale.
2. The index on the wafer backside (defined by the circle) is located above the index of the bump side (defined by the triangle/arrow).

Table 25. M95256-DR WLCSP, 0.5 mm pitch, package mechanical data

Symbol	Millimeters			Inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.600	0.550	0.650	0.0236	0.0217	0.0256
A1	0.245	0.220	0.270	0.0096	0.0087	0.0106
A2	0.355	0.330	0.380	0.0140	0.0130	0.0150
B	Ø 0.311			Ø 0.0122		
D	1.970	1.950	1.990	0.0776	0.0768	0.0783
E	1.785	1.765	1.805	0.0703	0.0695	0.0711
e	0.500			0.0197		
e1	0.866			0.0341		
e2	0.250			0.0098		
e3	0.433			0.0170		
F	0.552	0.502	0.602	0.0217	0.0198	0.0237
G	0.392	0.342	0.442	0.0154	0.0135	0.0174
N[2]	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. N is the total number of terminals.

11 Part numbering

Table 26. Ordering information scheme

Example: M95256 – W MN 6 T P /A

Device type

M95 = SPI serial access EEPROM

Device function

256 = 256 Kbit

256-D = 256 Kbit plus Identification page

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.8 to 5.5 V

Package

MN = SO8 (150 mils width)

DW = TSSOP8 (169 mils width)

CS = WLCSP

MB or MC = UFDFPN8 (MLP8)

Device grade

6 = Industrial temperature range, –40 to 85 °C. Device tested with standard test flow

3 = Device tested with High Reliability Certified Flow(1)

Automotive temperature range (–40 to 125 °C)

Option

blank = Standard packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHs compliant)

Process

A or AB = F8L(2)

K = F8H

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Used only for device grade 3 and WLCSP packages.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

12 Revision history

Table 27. Document revision history

Date	Revision	Changes
17-Nov-1999	2.1	New -V voltage range added (including the tables for DC characteristics, AC characteristics, and ordering information).
07-Feb-2000	2.2	New -V voltage range extended to M95256 (including AC characteristics, and ordering information).
22-Feb-2000	2.3	tCLCH and tCHCL, for the M95xxx-V, changed from 1µs to 100ns
15-Mar-2000	2.4	-V voltage range changed to 2.7-3.6V
29-Jan-2001	2.5	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Illustrations and Package Mechanical data updated
12-Jun-2001	2.6	Correction to header of Table 12B TSSOP14 Illustrations and Package Mechanical data updated Document promoted from Preliminary Data to Full Data Sheet
08-Feb-2002	2.7	Announcement made of planned upgrade to 10 MHz clock for the 5V, –40 to 85°C, range.
09-Aug-2002	2.8	M95128 split off to its own datasheet. Data added for new and forthcoming products, including availability of the SO8 narrow package.
24-Feb-2003	2.9	Omission of SO8 narrow package mechanical data remedied
26-Jun-2003	2.10	-V voltage range removed
21-Nov-2003	3.0	Table of contents, and Pb-free options added. -S voltage range extended to -R. V_{IL}(min) improved to –0.45V
17-Mar-2004	4.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices. Device grade information clarified
21-Oct-2004	5.0	M95128 datasheet merged back in. Product List summary table added. AEC-Q100-002 compliance. Device Grade information clarified. tHHQX corrected to tHHQV. 10MHz product becomes standard

Table 27. Document revision history (continued)

Date	Revision	Changes
13-Apr-2006	6	M95128 part numbers removed from document. PDIP8 package removed. *Delivery state* paragraph added. *Section 3.8: Operating supply voltage (VCC)* added and information removed below *Section 4: Operating features*. Power up state removed below *Section 6: Delivery state*. *Figure 18: SPI modes supported* modified and *Note 2* added. *Note 1* added to *Table 8*. I_{CC1} specified over the whole V_{CC} range and I_{CC0} added in *Table 14*, *Table 15* and *Table 16*. I_{CC} specified over the whole V_{CC} range in *Table 14*. *Table 17: AC Characteristics (M95256, Device Grade 6)* added. t_{CHHL} and t_{CHHH} replaced by t_{CLHL} and t_{CLHH}, respectively. *Figure 21: Hold timing* modified. *Process* added to *Table 25: Ordering information scheme*. *Note 1* added to *Table 25*. Note 1 removed from *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)*. T_A added to *Table 7: Absolute maximum ratings*. Order of sections modified.
15-Oct-2007	7	M95256 with device grade 6 temperature range removed. *Section 3.7: VSS ground* added, *Section 3.8: Operating supply voltage (VCC)* modified. Small text changes. *Section 5.4: Write Status Register (WRSR)*, *Section 5.5: Read from Memory Array (READ)* and *Section 6: Delivery state* updated. Note 2 below *Figure 17: Bus master and memory devices on the SPI bus* removed, replaced by explanatory paragraph. T_{LEAD} added to *Table 7: Absolute maximum ratings*. Test conditions modified for I_{CC0} and I_{CC1}, and V_{IH} min modified in *Table 17: AC characteristics (M95256, device grade 3)*. t_W modified and “preliminary data” note removed in *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)*. Blank option removed below Plating technology, process A modified and process V removed in *Table 25: Ordering information scheme*. *Table 26: Available M95256x products (package, voltage range, temperature grade)* added. SO8N and SO8W package specifications updated (see *Section 10: Package mechanical data*). Package mechanical data: inches calculated from mm and rounded to 3 decimal digits.
27-Mar-2008	8	*Section 3.8: Operating supply voltage (VCC)* modified. Small text changes. Frequency corrected *on page 1*. V_{IL} and V_{IH} modified in *Table 16: DC characteristics (M95256-R, M95256-DR, device grade 6)*. AB Process added to *Table 25: Ordering information scheme*.
15-Jul-2008	9	WLCSP package added (see *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)* and *Section 10: Package mechanical data*).

Table 27. Document revision history (continued)

Date	Revision	Changes
24-Jun-2010	10	M95256-DR part number added. Updated *Section 3.8: Operating supply voltage (VCC)* Updated *Section 4.3: Data protection and protocol control* Updated *Section 5.4: Write Status Register (WRSR)* Added note in *Section 5.6: Write to Memory Array (WRITE)* Updated *Table 7: Absolute maximum ratings* Added *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)* Updated *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)*
07-Sep-2010	11	Updated *Section 1: Description*. Updated *Section 5.7: Read Identification Page (available only in M95256-DR devices)*. Updated *Section 5.8: Write Identification Page*. Updated *Section 5.9: Read Lock Status (available only in M95256-DR devices)*.
12-Nov-2010	12	Updated *Features*. Updated *Section 5.8: Write Identification Page*. Added *Figure 25: TSSOP8 – 8 lead thin shrink small outline, package outline*. Added *Table 23: UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, package mechanical data*. Updated *Section 11: Part numbering*. Updated *Table 26: Available M95256x products (package, voltage range, temperature grade)*. Updated *Figure 25*, *Figure 26*.

Table 27. Document revision history (continued)

Date	Revision	Changes
22-Mar-2011	13	Deleted: – SO8 (MW) picture under *Features* – SO8 (MW) mechanical dimensions Updated: – UFDFPN8 (MB) with UFDFPN8 (MB, MC) picture under *Features* – *Section 5.6.1: ECC (error correction code) and Write cycling* – *Section 7: Connecting to the SPI bus* – *Table 7: Absolute maximum ratings* Process letter K substituted with only concerned products (M95256-D and M95256 in MLP8 package MC). – Rephrased “test condition” text in: *Table 14: DC characteristics (M95256, device grade 3)* *Table 15: DC characteristics (M95256-W, device grade 6)* *Table 16: DC characteristics (M95256-W, device grade 3)* *Table 17: DC characteristics (M95256-R, M95256-DR, device grade 6)* *Table 18: AC characteristics (M95256, device grade 3)* *Table 19: AC characteristics, M95256-W, device grade 6* *Table 20: AC characteristics (M95256-W, device grade 3)* *Table 21: AC characteristics (M95256-DR, M95256-R device grade 6)* Added: – Caution under *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)* – MC = UFDFPN8 package in *Section 11: Part numbering*
20-May-2011	14	Updated: – UFDFPN8 offered in only one package version Added: – *Table 13: Memory cell characteristics*
19-Jul-2011	15	MC package added (UFDFPN8)
23-Nov-2011	16	Updated: – Footnote 3 below *Table 7: Absolute maximum ratings* – Footnotes 1, 2, 4, 5 below *Table 15: DC characteristics (M95256-W, device grade 6)* – Footnotes 1, 2, 3, 5 below *Table 17: DC characteristics (M95256-R, M95256-DR, device grade 6)* – *Table 19: AC characteristics, M95256-W, device grade 6* headings, T_{QLQH} and T_{QHQL} values. One footnote removed and one added – *Table 21: AC characteristics (M95256-DR, M95256-R device grade 6)*, new columns for new pairs of products. Footnote 2 edited.
17-Jan-2012	17	Updated *Figure 25: UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline*.

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