PRODUCT INFORMATION LETTER

PIL AMS-APD/12/7302
Notification Date 06/18/2012

SO18 & SO 28 package lead frame swap from AMST to ASM.

Production process involved	Backend package assembly
Production process details	Generic
Reason for change	to qualify new lead frame
Description	SO18 and SO28 lead frame supply to move from AMST to ASM, due to sudden unexpected closure of AMST plant. ASM is already an existing qualified lead frame supplier of ST. Electrical, mechanical specifications, material composition & design of both SO 18 & SO 28 lead frame from ASM remain the same. SO28 is qualified and the report is as attached. The qualification for SO18 is in progress and the report will be available on request once completed.
Forecasted date of implementation	16-Jul-2012
Forecasted date of samples for customer	15-Jun-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Jun-2012
Description of qualification program	See Attached Qualification Plan
Involved ST facilities	ASM

DOCUMENT APPROVAL

Name	Function
Mcdonagh, Gary	Division Marketing Manager
Lisi, Giuseppe	Division Q.A. Manager
Italia, Francesco	Process Owner

Reliability Report

SO28 .30 WITH EMBEDDED CRYSTAL

New Frame: ASM
Assembly plant: Cirtek

T.V.: M41ST87WMX6E3 Line: D6AA61

General Information	
Product Line	D6AA61
Product Description	5.0 V and 3.3/3.0 V secure serial RTC and NVRAM supervisor with tamper detection and 128 bytes of clearable NVRAM
P/N	M41ST87W
Product Group	AMS
Product division	**Mixed Processes Division MSH**
Package	SO28 .30 with Embedded Crystal
Silicon Process technology	HCMOS4

Locations	
Wafer fab	Singapore
Assembly plant	Cirtek
Reliability Lab	**IMS-APM Catania Reliability Lab**
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	22-May-2012	9	Stefania Motta	Giovanni Presti	First Issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the new lead frame ASM in CIRTEK , for SO28 package, with Embedded Crystal using M41ST87 as TVs and applying the IR reflow profile (JL3) at Tpeak=260C

3.2 Conclusion

Reliability tests have shown that the devices behave correctly against environmental tests (no failure) until the final step. Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The M41ST87Y/W secure serial RTC and NVRAM supervisor is a low power 1280-bit, static CMOS SRAM organized as 160 bytes by 8 bits. A built-in 32.768 kHz oscillator (internal crystal-controlled) and 8 bytes of the SRAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 11 bytes of RAM provide calibration, status/control of alarm, watchdog, tamper, and square wave functions. 8 bytes of ROM and finally 128 bytes of user RAM are also provided. Addresses and data are transferred serially via a two line, bidirectional I2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41ST87Y/W has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a small lithium button-cell supply when a power failure occurs.
Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, tamper detection, watchdog timer, and programmable square wave output. Other features include a power-on reset as well as two additional debounced inputs (RSTIN1 and RSTIN2) which can also generate an output reset (RST). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year), 30 and 31 day months are made automatically.

4.2 Construction note

	P/N M41ST87
Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6 6" Singapore
Technology	HCMOS4
Process family	HCMOS4_P/CU
Die finishing back side	RAW SILICON - BACK GRINDING
Die size	2.880 x 4.520mm
Bond pad metallization layers	Ti/AlSiCu/TiN
Passivation type	PSG+Silicon Nitride+Polyimide
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Asia Pac Singapore EWS
Tester	Teradyne J750
Assembly information	
Assembly site	CIRTEK - PHILLIPINES
Package description	SO28 .30 WITH EMBEDDED CRYSTAL
Molding compound	**EME-6650RL**
Frame material	Copper (C-194)
Die attach process	Glue dispense
Die attach material	Ablebond 84-1 LMIS R4
Die pad size	0.140 x 0.205 inch
Wire bonding process	Eutectic wirebond, crystal welding
Wires bonding materials/diameters	**Au wire, 1.3mil**
Final testing information	
Testing location	ST Muar
Tester	J750
Test program	J750-PBHLB83X-071_09_00

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Package	Product Line	Comments
1	V61396T4	9133C01	SO28 .30 WITH EMBEDDED CRYSTAL	D6AA61	MicroCrystal,40kOhm MS3V-T1N, 12.5pF, #201820-BA01 **New ASM Frame**

5.2 Test plan and results summary

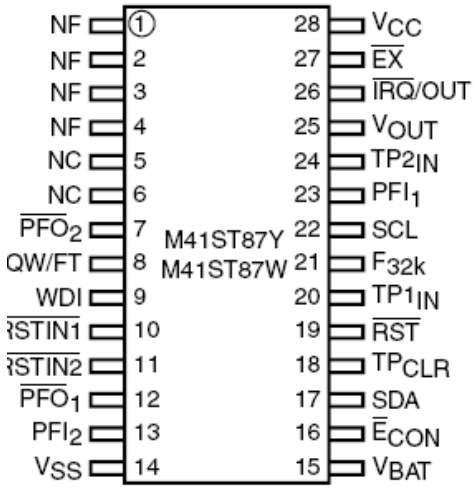
P/N M41ST87

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			note
						Lot	Lot	Lot	
Die Oriented Tests									
HTS	N	JESD22 A-103	Tj = 150℃	45	1000 H	0/45			
Package Oriented Tests									
PC(1)		JESD22 A-113	**Drying 24 H @ 125℃ Store 48 H @ Ta=60℃ Rh=60% Oven Reflow @ Tpeak=245℃ 3 times**	210	Final	Pass	Pass	Pass	
PC(2)		JESD22 A-113	**Drying 24 H @ 125℃ Store 48 H @ Ta=60℃ Rh=60% Oven Reflow @ Tpeak=260℃ 3 times**	210	Final	Pass	Pass	Pass	
AC(1)	Y	JESD22 A-102	Pa=2Atm / Ta=121℃ **After PC(1) @ 245℃**	50	96 H	0/50			
AC(2)	Y	JESD22 A-102	Pa=2Atm / Ta=121℃ **After PC(2) @ 260℃**	50	96 H	0/50			
TC(1)	Y	JESD22 A-104	Ta = -40℃ to 125℃ **After PC(1) @ 245℃**	50	500 cy	0/50			
TC(2)	Y	JESD22 A-104	Ta = -40℃ to 125℃ **After PC(2) @ 260℃**	50	500 cy	0/50			
THS(1)	Y	JESD22 A-101	Ta = 85℃, RH = 85% **After PC(1) @ 240℃**	50	1000 H	0/50			
THS(2)	Y	JESD22 A-101	Ta = 85℃, RH = 85% **After PC(2) @ 260℃**	50	1000 H	0/50			

6 ANNEXES

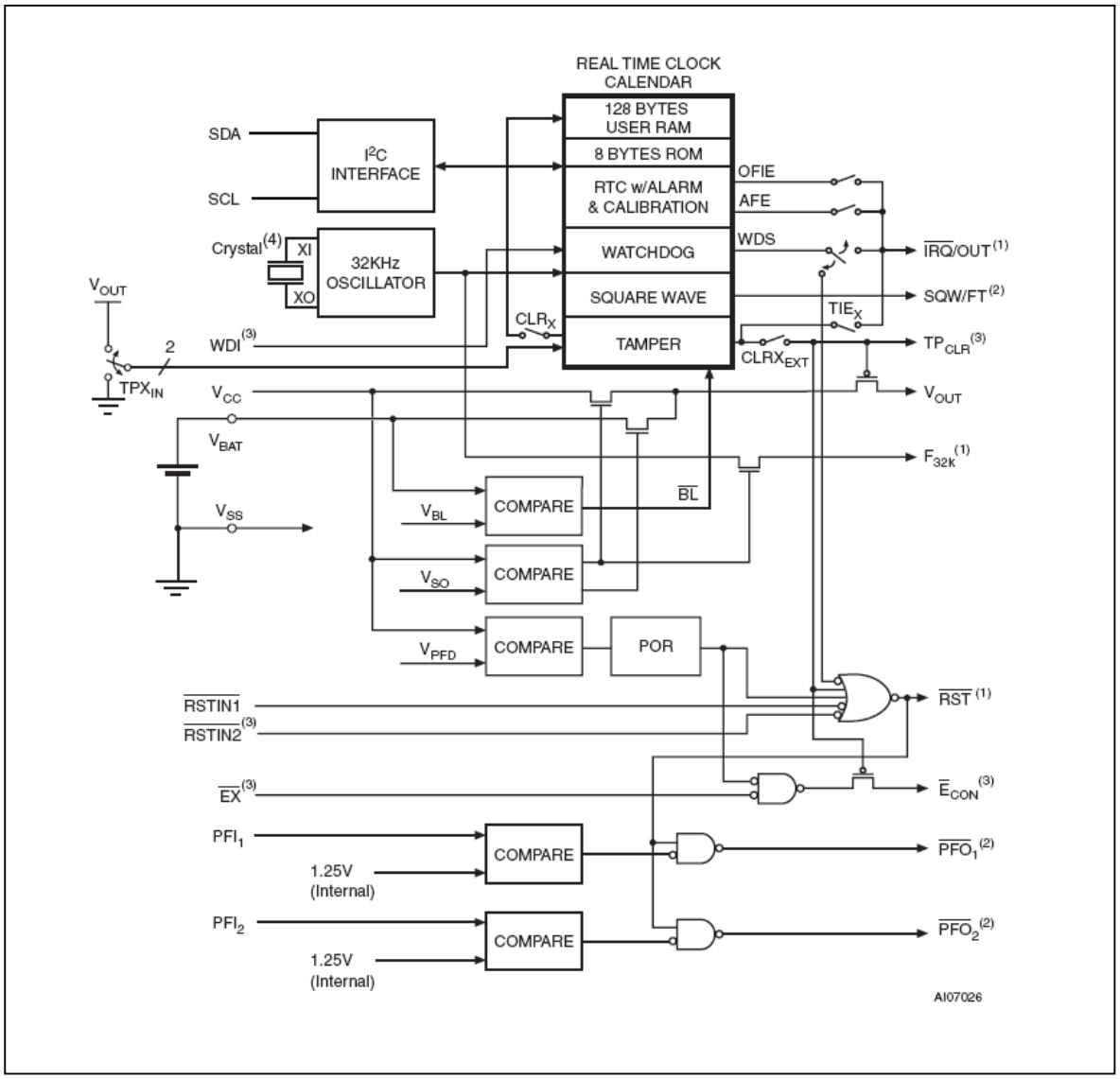
6.1 Device details

6.1.1 Pin connection



XI(1)	Oscillator input
XO(1)	Oscillator output
$\overline{E}_{CON}$(2)	Conditioned chip enable output
$\overline{EX}$(2)	External chip enable
$\overline{IRQ}$/OUT(3)	Interrupt/out output (open drain)
PFI_1	Power fail input 1
PFI_2	Power fail input 2
$\overline{PFO}_1$(4)	Power fail output 1
$\overline{PFO}_2$(4)	Power fail output 2
$\overline{RST}$(3)	Reset output (open drain)
$\overline{RSTIN1}$	Reset 1 input
$\overline{RSTIN2}$(2)	Reset 2 input
SCL	Serial clock input
SDA	Serial data input/output
SQW/FT(4)	Square wave output/frequency test
WDI(2)	Watchdog input
V_{CC}	Supply voltage
V_{OUT}	Voltage output
V_{SS}	Ground
F_{32k}(3)	32 kHz square wave output (open drain)
$TP1_{IN}$	Tamper pin 1 input
$TP2_{IN}$	Tamper pin 2 input
TP_{CLR}(2)	Tamper pin RAM clear
V_{BAT}	Positive battery pin input
NF(5)	No function
NC(5)	No connect

6.1.2 Block diagram

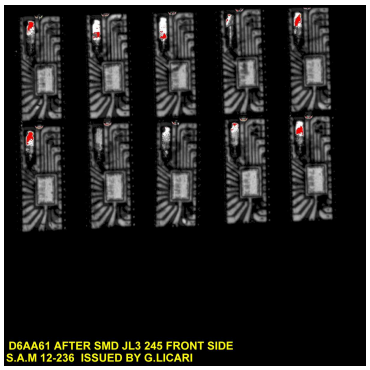


6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. Temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance, corrosion is put in evidence.

6.3 Pictures related to reliability tests

SAM ANALYSIS

PC(1) JL3 @245℃	
	
FIG.1: Dut before SMD JL3 @ 245℃, no die surface-molding compound delamination evidence REF.: S.A.M. 12- 234	FIG.2: Dut after SMD JL3 @ 245℃, no die surface-molding compound delamination evidence REF.: S.A.M. 12-236

PC(2) JL3 @260℃	
	
FIG.1: Dut before SMD JL3 @ 260℃, no die surface-molding compound delamination evidence REF.: S.A.M. 12- 233	FIG.2: Dut after SMD JL3 @ 260℃, no die surface-molding compound delamination evidence REF.: S.A.M. 12-235

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