DIODES INCORPORATED

www.diodes.com

Diodes Incorporated for Discrete and Analog Semiconductors

QPAK/PPAP – 11102601

Qualification Report

PCN-2078

Manufacturer No.:	**PCN-2078 – Qualification of Die Shrink**
Revision	**0**
Date:	**July 23, 2012**
Qualified By:	**Shanghai Kaihong Electronic Co., Ltd. & Diodes Shanghai Co., Ltd.**
Also Applicable To:	**The part numbers listed in the associated PCN are Qualified by Similarity (QBS) to the devices included in this report.**

Please go to www.diodes.com for current device data sheets.

Prepared By:	**Diodes US Document Control**	**Date**	**July 23, 2012**
Approved By:	**Diodes US QRA Department**	**Date**	**July 23, 2012**

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DIODES INCORPORATED
4949 Hedgcoxe Road, Suite # 200, Plano, TX 75024 USA
www.diodes.com

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Plastic encapsulated Diodes Incorporated semiconductor devices are not designed and are not warranted to be suitable for use in some military applications and/or military environments. Use of plastic encapsulated Diodes Incorporated semiconductor devices in military applications and/or military environments, in lieu of hermetically sealed ceramic devices, is understood to be fully at the risk of Buyer.

Quality and reliability data provided by Diodes Incorporated is intended to be an estimate of product performance based upon history only. It does not imply that any performance levels reflected in such data can be met if the product is operated outside the conditions expressly stated in the latest published data sheet for a device.

Existing industry standards for plastic encapsulated microcircuit qualification and reliability monitors are based upon historical data, experiments, and field experience with the use of these devices in commercial and industrial applications. The applicability of these standards in determining the suitability for use and safety performance in life support, military and aerospace applications has not been established. Due to the multiple variations in field operating conditions, a component manufacturer can only base estimates of product life on models and the results of package and die level qualification. The buyer's use of this data, and all consequences of such use, is solely the buyer's responsibility. Buyer assumes full responsibility to perform sufficient engineering and additional qualification testing in order to properly evaluate the buyer's application and determine whether a candidate device is suitable for use in that application. The information provided by Diodes Incorporated shall not be considered sufficient grounds on which to base any such determination.

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DIODES INCORPORATED
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Plano, TX 75024 USA
(972) 987-3900
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DATE: 23rd July, 2012

PCN #: 2078

PCN Title: Qualification of Die Shrink

Dear Customer:

This is an announcement of change(s) to products that are currently being offered by Diodes Incorporated.

We request that you acknowledge receipt of this notification within 30 days of the date of this PCN. If you require samples for evaluation purposes, please make a request within 30 days as well. Otherwise, samples may not be built prior to this change. Please refer to the implementation date of this change as it is stated in the attached PCN form. Please contact your local Diodes sales representative to acknowledge receipt of this PCN and for any sample requests.

The changes announced in this PCN will not be implemented earlier than 90 days from the notification date stated in the attached PCN form.

Previously agreed upon customer specific change process requirements or device specific requirements will be addressed separately.

For questions or clarification regarding this PCN, please contact your local Diodes sales representative.

Sincerely,

Diodes Incorporated PCN Team

PRODUCT CHANGE NOTICE PCN-2078 REV00

Notification Date:	Implementation Date:	Product Family:	Change Type:	PCN #:
23rd July, 2012	21st October, 2012	Select Discrete Devices	Wafer FAB Material	**2078**

TITLE
Qualification of Die Shrink

DESCRIPTION OF CHANGE
In order to assure continuity of supply, this PCN is being issued to notify customers of a qualified shrink die from the existing wafer fabrication source (Diodes internal FabTech Inc. - KFAB) for the parts listed in the attached table. Full electrical characterization and high reliability testing has been completed on representative parts to ensure no change to device functionality or data sheet electrical specifications.

IMPACT
None

PRODUCTS AFFECTED
Please see attached table

WEB LINKS	
Manufacturer's Notice:	http://www.diodes.com/quality/pcns
For More Information Contact:	http://www.diodes.com/contacts
Data Sheet:	http://www.diodes.com/products

DISCLAIMER
Unless a Diodes Incorporated Sales representative is contacted in writing within 30 days of the posting of this notice, all changes described in this announcement are considered approved.

PCN-2078 Part List

BAT54-13-F
BAT54-7-F
BAT54A-13-F
BAT54A-7-F
BAT54ADW-7-F
BAT54AT-7-F
BAT54ATA
BAT54AW-7-F
BAT54BRW-7-F
BAT54C-7-F
BAT54CDW-13-F
BAT54CDW-7-F
BAT54CT-7-F
BAT54CTA
BAT54CW-13-F
BAT54CW-7-F
BAT54DW-7-F
BAT54JW-7-F
BAT54LP-7
BAT54LPS-7
BAT54S-7-F
BAT54ST-7-F
BAT54STA
BAT54SW-7-F
BAT54T-7-F
BAT54TA
BAT54TW-7-F
BAT54V-7
BAT54W-13-F
BAT54W-7-F
BAT54WS-7-F
BAT54WT-7

DIODES INCORPORATED

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130C
DIC P/N	BAT54LP-7	**Lead material type**	C7025HH
Package Type	DFN1006-2	**Lead Material manufacturer**	MHT/ASM/PBE
DIE P/N	S9069Q	**Lead plating/ coating**	NiPdAu
Die line or process	Sky	**Lead frame material type**	C7025HH
Wafer Diameter	5 inch	**Header plating (Die land area)**	NiPdAu
Wafer Fab Site(s)	DFT	**Max junction temperature(T_j)**	125C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	320 ℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi
Die attach Method / Material	Epoxy/QMI519	**Front metal thickness (Top layer)**	2um
Bond wire material & dia.	Gold wire, 0.7mil	**Back metal type (All layers)**	TiAu
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	0.5um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.31*0.31*0.14
Package material type	EME-G770HCD	**Die passivation thickness range**	6000A to 9000A
Package material manufacturer	Sumitomo	**No. of mask steps**	3

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Caixia Wei	November 4, 2011	Robin Sun	November 4, 2011
Signature				
Title	SBR PE	November 4, 2011	Discrete Manager	Nov 4，2011

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAT54LP SWR1111123 CUSTOMER: Package:DFN1006-2 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer S9069Q qual,0.7Au				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=100uA Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=100mA Characteristic IR @VR=30V Characteristic IR @VR=25V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/25	1.7A
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=24V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=24V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=24V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=24V				
	Pretest		1	77	0/77	
	@ 500 Hours	T=85*C RH=85% Vr=24V	1	77	0/77	
	@ 1000 Hours	T=85*C RH=85% Vr=24V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=200mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	320 ℃/W
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 2/3/12		Approved by:Adam Gu 2/3/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160C
DIC P/N	BAT54WS-7-F-76	**Lead material type**	Alloy 42
Package Type	SOD-323	**Lead Material manufacturer**	MHT/VAST/XMYH/NBKQ
DIE P/N	S9069	**Lead plating/ coating**	Pure Sn
Die line or process	Sky	**Lead frame material type**	SOD323A
Wafer Diameter	5 inch	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	DFT	**Max junction temperature(T_j)**	150C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	248 ℃/W
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	578 ℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al/Si
Die attach Method / Material	EUTECTIC / N/A	**Front metal thickness (Top layer)**	2um
Bond wire material & dia.	Cu wire, 1.0mil	**Back metal type (All layers)**	AuNi
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	0.5um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.31*0.31*0.21
Package material type	KTMC1050G	**Die passivation thickness range**	6000A to 9000A
Package material manufacturer	KCC	**No. of mask steps**	3

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

vcxbb

Completed by		Date	Certified by	Date
Typed/Printed	Caixia Wei	November 4, 2011	Robin Sun	November 4, 2011
Signature				
Title	SBR PE	November 4, 2011	Discrete Manager	November 4, 2011

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAT54WS SWR1111030 CUSTOMER: Package:SOD323 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer S9069 qual,1.0Cu				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=100uA Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=100mA Characteristic IR @VR=30V Characteristic IR @VR=25V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/25	2.2A
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=24V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=24V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=24V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=24V			N/A	
	Pretest		1	77		
	@ 500 Hours	T=85*C RH=85% Vr=24V	1	77		
	@ 1000 Hours	T=85*C RH=85% Vr=24V	1	77		
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=24V	1	77	0/77	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=200mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	578 ℃/W
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 2/1/12		Approved by:Adam Gu 2/1/12				