PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ANALOG MEMS SENSORS/24/14698
1.3 Title of PCN	Additional capacity for HF5CMOS in ST Crolles
1.4 Product Category	See product list
1.5 Issue date	2024-04-11

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	PIKE EMMA
2.1.2 Phone	+44 1628896111
2.1.3 Email	emma.pike@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication (SOP 2617)	Front end plant : - Current : UMC Taiwan - New : ST Crolles

4. Description of change		
	Old	New
4.1 Description	Front end plant : - UMC Taiwan	Front end plant : - UMC Taiwan - ST Crolles
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	Progressing on the activities related to HF5CMOS technologies manufacturing double sourcing, ST is glad to announce additional production site in ST Crolles (France) for selected products. This process is already running in ST Crolles since 2014 for similar products.
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
6.1 Description	New Finished good codes

7. Timing / schedule	
7.1 Date of qualification results	2024-04-09
7.2 Intended start of delivery	2024-07-20
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14698 14698- PCN_Qual_ReportV9XX_UMCtoCrolles.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-04-11

9. Attachments (additional documentations)
14698 Public product.pdf 14698 14698- PCN_Qual_ReportV9XX_UMCtoCrolles.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	TSL6201ILT	
	TSV911AIDT	
	TSV911AILT	
	TSV911ILT	

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Subject to any contractual arrangement in force with you or to any industry standard implemented by us, STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Additional capacity for HF5CMOS in ST Crolles

PCN Reference : ANALOG MEMS SENSORS/24/14698

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TSL6202IST	TSV911AIDT	TSV911AILT
TSL6204IPT	TSL6201ILT	TSV911ILT
TSV911RILT	TSV911IDT	

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Subject to any contractual arrangement in force with you or to any industry standard implemented by us, STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

PRODUCT/PROCESS
CHANGE NOTIFICATION
ANALOG MEMS SENSORS/24/14698

Analog, Power&discrete, MEMS and Sensor Group
Additional capacity for additional HF5CMOS

UMC Taiwan

ST Crolles & UMC Taiwan

WHAT:

Progressing on the activities related to HF5CMOS technologies manufacturing double sourcing, ST is glad to announce additional production site in ST Crolles (France) for selected products. This process already running in ST Crolles Since 2014 for similar products.

Material	Current process	additional process	Comment
diffusion location	UMC Taiwan	ST Crolles	
Wafer dimension	8 inches	8 inches	No change
Metallization	AlCu	AlCu	No change
Passivation	PSG/Nitride	PSG/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

For the complete list of part numbers affected by the change, please refer to the attached Product list.

Samples are available, upon request.

WHY:
To improve service to ST Customers and increase capacity for the affected technologies.

HOW:
HF5CMOS process already qualified in ST Crolles for other products. Extension of the line for additional AMS products is qualified based on qualification plan here attached.
Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Reliability evaluation plan for all the details.

WHEN:
Production in ST Crolles for selected products, is forecasted in July 2024.

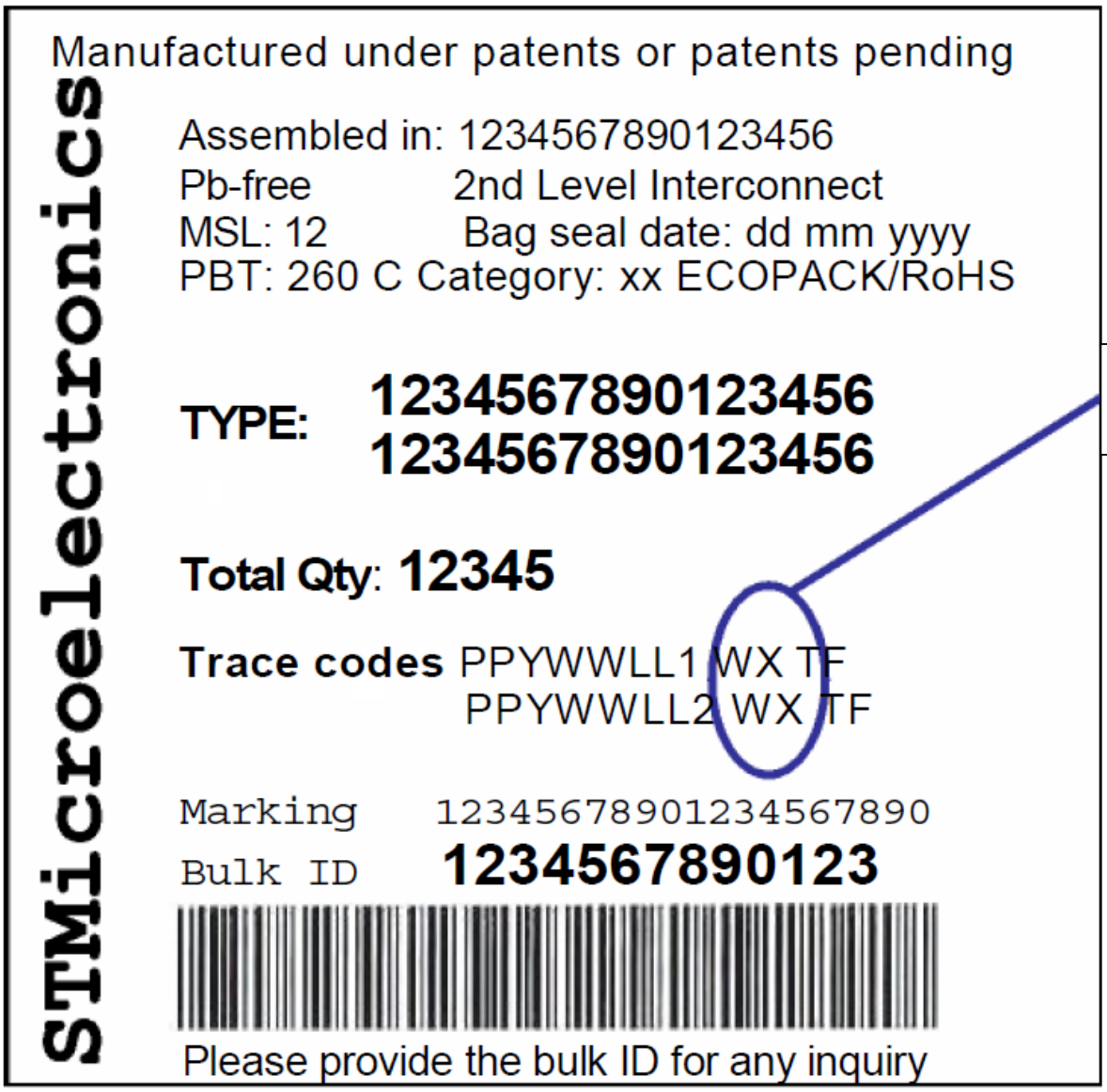
Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by datecode and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Shipments from new Wafer FAB location will be tracked on the ST Standard Label as showed below:



Generic ST Standard label

Change Qualification Plan

Double source front end plant qualification
ST Crolles HCMOS5 and HCMOS 6

Test vehicle	
Product Lines:	*V911, V912, V914, 3021*
Product Families:	• Single, dual, and quad rail-to-rail input/output 8 MHz operational amplifiers • Rail-to-rail 1.8 V high-speed comparator
P/Ns:	*TSV911ILT, TSL6202IST, TSL6204IP, TS3021ILT*
Product Groups:	*AMS*
Product Divisions:	*General Purpose Analog*
Packages:	*Sot23-5, MiniSO, TSSOP14*
Silicon Process techn.:	*HF5CMOS*

Locations	
Wafer Diffusion Plants:	*ST Crolles 200*
EWS Plants:	*ST Singapore*
Assembly Plants:	*Carsem Malaysia, ST Bouskoura (Morocco),, TSHT (China), Amkor Philippines*
T&F Plants:	*Carsem Malaysia, ST Bouskoura (Morocco),, TSHT (China) Amkor Philippines*

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q006	Guidelines for Characterizing the Electrical Performance of IC Products

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 QUALIFICATION EVALUATION OVERVIEW

3.1 Objectives

To Qualify additional products (V9XX) in HF5CMOS in ST Crolles.

3.2 Conclusion

Qualification Plan requirements must be fulfilled without exception. It is stressed that reliability tests must show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 CHANGE CHARACTERISTICS

4.1 Change description

Additional source for Selected products in HF5CMOS in ST Crolles

4.2 Change details

Material	Current process	additional process	Comment
diffusion location	UMC Taiwan	ST Crolles	
Wafer dimension	8 inches	8 inches	No change
Metallization	AlCu	AlCu	No change
Passivation	PSG/Nitride	PSG/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

4.3 Test vehicles description

	P/N TSV911ILT	P/N TSV912IDT	P/N TSL6202IST		P/N TSL6204IPT
Wafer/Die fab. information					
Wafer fab manufacturing location	Crolles 200	Crolles 200	Crolles 200		Crolles 200
Technology	HF5CMOS	HF5CMOS	HF5CMOS		HF5CMOS
Process family	HF5CMOS	HF5CMOS	HF5CMOS		HF5CMOS
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON		RAW SILICON
Die size (microns)	850x950µm²	1100x1070µm²	1100x1070µm²		
Bond pad metallization layers	AlCu	AlCu	AlCu		AlCu
Passivation type	PSG + NITRIDE	PSG+Nitride+PIX	PSG + NITRIDE		PSG + NITRIDE
Wafer Testing (EWS) information					
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore		ST Singapore
Assembly information					
Assembly site	Carsem Malaysia	ST Bouskoura	TSHT	Amkor Ph.	ST Bouskoura
Package description	Sot23-5	SO8	MiniSO8	MiniSO8	TSSOP14
Molding compound	Hitachi CEL8240HF	Sumitomo G700KC	Hitachi CEL-9220HF	Sumitomo G700LS	Sumitomo G700KC
Frame material	Copper	Copper	Copper	Copper	Copper
Die attach process	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue
Die attach material	QMI519	Epoxy 8601S-25	8200T Henkel	ABLESTICK 8290	Epoxy 8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Gold wire 1 mil	Copper wire 1 mil	CuPd wire 1 mi	Gold 0.8mils	Copper wire 1 mil
Lead finishing process	Preplated frame	Electroplating	Electroplating	Preplated frame	Preplated frame
Lead finishing/bump solder material	NiPdAu Pre-plated	Sn	Sn	NiPdAu Pre-plated	NiPdAu Pre-plated
Final testing information					
Testing location	Carsem Malaysia	ST Bouskoura	TSHT	Amkor Ph.	ST Bouskoura

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	P/N	Process/ Package	Comments
1	TSV911ILT	HF5CMOS/Sot23-5	
2	TSV912IDT	HF5CMOS/SO8	
3	TSV912IDT	HF5CMOS/SO8	
4	TSV912IDT	HF5CMOS/SO8	
5	TSL6202IST	HF5CMOS/MiniSO8	TSHT
6	TSL6202IST	HF5CMOS/MiniSO8	Amkor Ph
7	TSL6204IPT	HF5CMOS/TSSOP14	

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS							Note
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot7	
Die Oriented Tests													
HTB High Temp. Bias	N	JESD22 A-108	Tj = 125°C, BIAS	77	168H 500H 1000H	0/77 w14	W22 W26	W22 W26	W22 W26	0/77 0/77	0/77 0/77	0/77 0/77 0/77	
HTSL High Temp. Storage Life	N	JESD22 A-103	Ta = 150°C	77	500H 1000 H	0/77 0/77	W20 W24	W18 W22	W18 W22	0/77 0/77	0/77 0/77	0/77 0/77	
ELFR Early Life Failure Rate	N	AEC Q100 - 008	Ta=125°C	800	48H	0/800				0/800	0/800	0/800	
Package oriented test													
PC Preconditioning		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	PASS	W19	W17	W17	PASS	PASS	PASS	
UHAST Unbiased humidity accel-erated stress	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H	W17	W20	W18	W18	0/77	0/77	0/77	
TC Temperature Cycling	Y	JESD22 A-104	Ta = -65°C to 150°C	77	500cy 1000cy 2000cy	W19 W25 W34	W21 W23 W27	W21 W26 W35	W21 W26 W35	0/77 0/77 w13	0/77 w15 w23	0/77 0/77 w15	
THB Temperature Humidity Bias	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS	77	168H 500 H 1000 H	0/77 w13 w17	W22 W26	W22 W26	W22 W26	0/77 w13	0/77 0/77 w12	0/77 0/77	
Other Tests													
ESD Electro Static Discharge	-	AEC Q101-001, 002 and 005	HBM	3		0/3	W20			0/3	0/3	0/3	
			CDM	3		0/3	W20			0/3	0/3	0/3	
LU Latch up	N	AEC Q100-004	LU	6		0/6	W20			0/6	0/6	0/6	

ANNEXES

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Test name	Description	Purpose
PTC Power & Temperature Cycling	The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.	It is intended to simulate worst case conditions encountered in typical applications. Typical failure modes are related to parametric limits and functionality. Mechanical damage such as cracking, or breaking of the package will also be considered a failure provided such damage was not uinduced by fixturing or handling.
EV External Visual	Inspect device construction, marking and workmanship	To verify visual defects on device (form, marking,…).
LI Lead Integrity	Various tests allow determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly.	This test is applicable to all throughhole devices and surface-mount devices requiring lead forming by the user.
WBP Wire Bond Pull	The wire is submitted to a pulling force (approximately normal to the surface of the die) able to achieve wire break or interface separation between ball/pad or stitch/lead.	To investigate and measure the integrity and robustness of the interface between wire and die or lead metallization
WBS Wire Bond Shear	The ball bond is submitted to a shear force (parallel to the pad area) able to cause the separation of the bonding surface between ball bond and pad area.	To investigate and measure the integrity and robustness of the bonding surface between ball bond and pad area.
DS Die Shear	This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.	The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates.
PD Physical Dimension	All physical dimension quoted in datasheet of the device are measured.	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
SD Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.