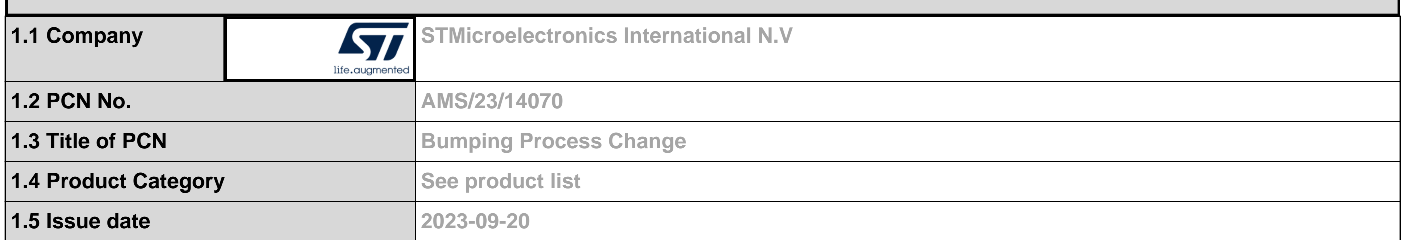
PRODUCT / PROCESS CHANGE NOTIFICATION



1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMS/23/14070
1.3 Title of PCN	Bumping Process Change
1.4 Product Category	See product list
1.5 Issue date	2023-09-20

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	NEMETH KRISZTINA
2.1.2 Phone	+49 89460062210
2.1.3 Email	krisztina.nemeth@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	ASE Taiwan

4. Description of change		
	Old	New
4.1 Description	Printing Bumping Process (ASE, Taiwan)	Plating Bumping Process (SCS =Stats Chippac Singapore)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact on the Electrical, Mechanical, Quality and Reliability Characteristics.	

5. Reason / motivation for change	
5.1 Motivation	Following ASE communication about the termination of the current Printing Bumping Process, ST plans to qualify and implement a New Bumping Process in SCS (Stats Chippac Singapore) OSAT. No change to the Package Outline Assembly (mechanical) and electrical characteristics (datasheet). No other change is made with respect to this PCN. Wafer diffusion as well as Testing & Finishing/ DPS remain unchanged both in terms of flow and location.
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	The traceability of the new parts will be ensured by physical Die Level and Lot Level codification.

7. Timing / schedule	
7.1 Date of qualification results	2023-08-28
7.2 Intended start of delivery	2023-11-30
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14070 ReliabilityEvaluationReport-V788_V1.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-09-20

9. Attachments (additional documentations)
14070 Public product.pdf 14070 ReliabilityEvaluationReport-V788_V1.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STC3115AIJT	

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Internal Reliability Evaluation Report

Bumping transfer from ASE to JCET plant line V78801

General Information	
Product Line	V78801
Product Description	Gas gauge IC with alarm output
P/N	GG25LJ
Product Group	AMG
Product division	GPA&RF
Package	CSPS0.4 BP 5-16
Silicon Process technology	HCMOS9A

Locations	
Wafer fab	Crolles 200
Bumping plant	STEF-JCET SCS
DPS plant	ST Shenzhen
Reliability Lab	ST Grenoble/ ST Shenzhen

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	04-05-2023		Claudine Larato		Initial version

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this qualification is to qualify the transfer of Bumping Process from ASEKH to JCET.
Following ASE communication about the termination of the current Printing Bumping Process by JULY 2023, STC3115AIJT$KDC, STC3115IJT$KDE should qualify and implement a new bumping process.
The new Bumping process will be implemented in SCS (Stats Chippac Singapore) OSAT.
No change to the Package Outline Assembly (mechanical) and electrical characteristics (datasheet). No other change is made with respect to this PCN.
Wafer diffusion as well as Testing & Finishing/ DPS remain unchanged both in terms of flow and location.
The packages under qualification is the CSPS0.4 BP 5-16.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Reliability agreement for the maturity 30 level is done for this V78801 line qualification.

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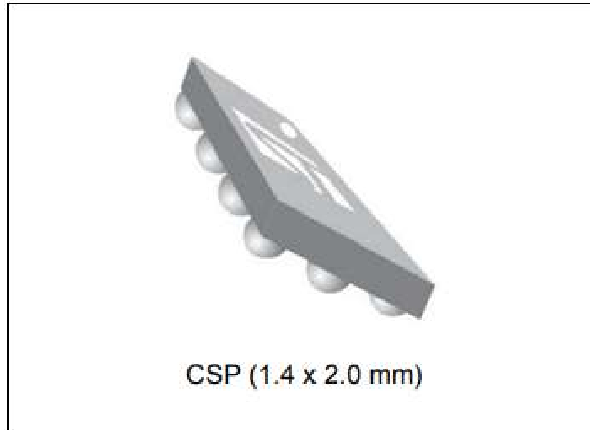
4 DEVICE CHARACTERISTICS

4.1 Device description


CSP (1.4 x 2.0 mm)

Features

- OptimGauge™ algorithm
- 0.25% accuracy battery voltage monitoring
- Coulomb counter and voltage-mode gas gauge operations
- Robust initial open-circuit-voltage (OCV) measurement at power up with debounce delay
- Low battery level alarm output with programmable thresholds
- Internal temperature sensor
- Battery swap detection
- Low power: 45 µA in power-saving mode, 2 µA max in standby mode
- 1.4 x 2.0 mm 10-bump CSP package

Applications

- Wearable
- Fitness and healthcare
- Portable medical equipment

Description

The GG25L includes the hardware functions required to implement a low-cost gas gauge for battery monitoring. The GG25L uses current sensing, Coulomb counting and accurate measurements of the battery voltage to estimate the state-of-charge (SOC) of the battery. An internal temperature sensor simplifies implementation of temperature compensation.

An alarm output signals a low SOC condition and can also indicate low battery voltage. The alarm threshold levels are programmable.

The GG25L offers advanced features to ensure high performance gas gauging in all application conditions.

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4.2 Construction note

	New Plant Qualification
	P/N LM358DT
Wafer/Die fab. information	
Wafer fab manufacturing location	CROLLES 200
Process FE technology	HCMOS9A
Die finishing back side	Raw Silicon
Die size	2040 x 1400 µm²
Bond pad metallization layers	Ti/NiCu/Au
Passivation type	PSG + NITRIDE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	
Tester	
Test program	
Assembly information	
Bumping site	TEF-JCET SCS
Package description	CSPS0.4 BP 5-16 fan-in
Bump process	Fan-in LeadFree balls Cu-RDL
Bump material	SAC105N 250um
repassivation	HD4100
UBM seed layer	Sputter Ti/CU
UBM	Cu electro-plating
DPS site	ST Shenzhen
Final testing information	
Testing location	
Tester	
Test program	

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5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
Lot 1	VJ222SYC /		GK243B9601 / GK243B96	1KN5*V7881DJ	CSPS0.4 BP 5-16	
Lot 2	VJ222SYC /		GK243B9602 / GK243B96	1KN5*V7881DJ	CSPS0.4 BP 5-16	
Lot 3	VJ222SYC /		GK243B9603 / GK243B96	1KN5*V7881DJ	CSPS0.4 BP 5-16	

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

P/N GG25LJ

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC		24h bake @ 125°C 168h @ 85°C / 85% RH 3 Reflows with standard JEDEC profile @ 260°C peak On single parts Visual Inspection	3	22	66	Lot 1 0/22 Lot 2 0/22 Lot 3 0/22	
HTSL	JESD22-A103	Ta= 150°C Duration= 1000hrs On Chip Board No Preconditioning Testing at Room	3	80	240	Lot 1 1000h : 0/80 Lot 2 1000h : 0/80 Lot 3 1000h : 0/80	
TC	JESD22-A104	Ta= -55°C / 150°C Cyc= 1000cy On Chip Board No Preconditioning Testing at Room	3	80	240	Lot 1 1000cy : 0/80 Lot 2 1000cy : 0/80 Lot 3 1000cy : 0/80	
THB	JESD22-A101	Ta= 85°C/85%RH Biased Duration= 1000hrs On Chip Board No Preconditioning Testing at Room	3	80	240	Lot 1 1000h : 0/80 Lot 2 1000h : 0/80 Lot 3 1000h : 0/80	

In case of rejects include a short description of the failure analysis and corrective actions.

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6 ANNEXES

6.1 Device details

6.1.1 Pin connection

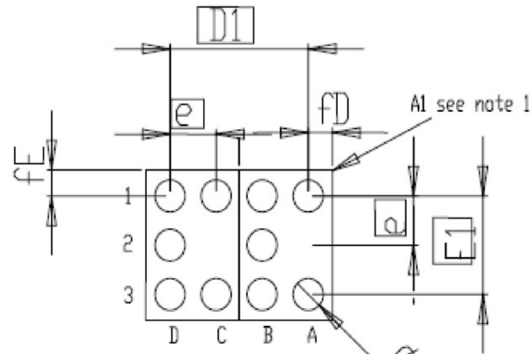

Table 2. GG25L pin description

Pin n°	CSP bump	Pin name	Type(1)	Function
1	A1	ALM	I/OD	Alarm signal output, open drain, external pull-up with resistor
2	B1	SDA	I/OD	I²C serial data
3	C1	SCL	I_D	I²C serial clock
4	D1	GND	Ground	Analog and digital ground
5	D2	NC	-	NC
6	D3	CG	I_A	Current sensing input
7	C3	RSTIO	I/OD	Reset sense input & reset control output (open drain)
8	B2	BATD/CD	I/OA	Battery charge inhibit (active high output) Battery detection (input)
9	B3	VCC	Supply	Power supply
10	A3	VIN	I_A	Battery voltage sensing input

1. I = input, 0 = output, OD = open drain, A = analog, D = digital, NC = not connected

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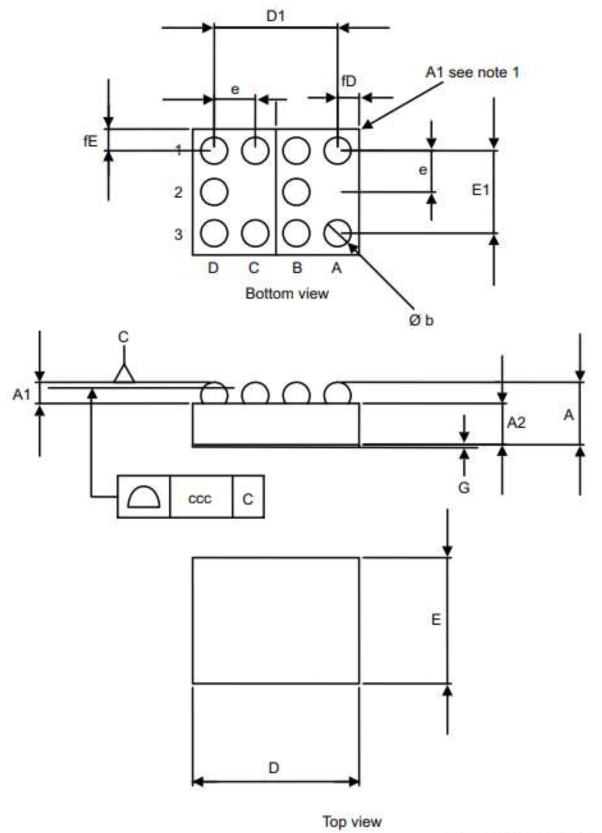
6.1

Table 16. Flip Chip CSP 1.4 x 2.04 mm package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.545	0.600	0.655	0.021	0.024	0.026
A1	0.165	0.200	0.235	0.006	0.008	0.009
A2	0.330	0.350	0.370	0.013	0.014	0.015
b	0.220	0.260	0.300	0.009	0.010	0.012
D	1.98	2.01	2.04	0.078	0.079	0.080
D1		1.20			0.047	
E	1.34	1.37	1.40	0.053	0.054	0.055
E1		0.800			0.031	
e	0.360	0.400	0.440	0.014	0.016	0.017
fD	0.395	0.405	0.415	0.016	0.016	0.016
fE	0.275	0.285	0.295	0.011	0.011	0.012
G		0.050			0.002	
ccc			0.050			0.002



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6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.

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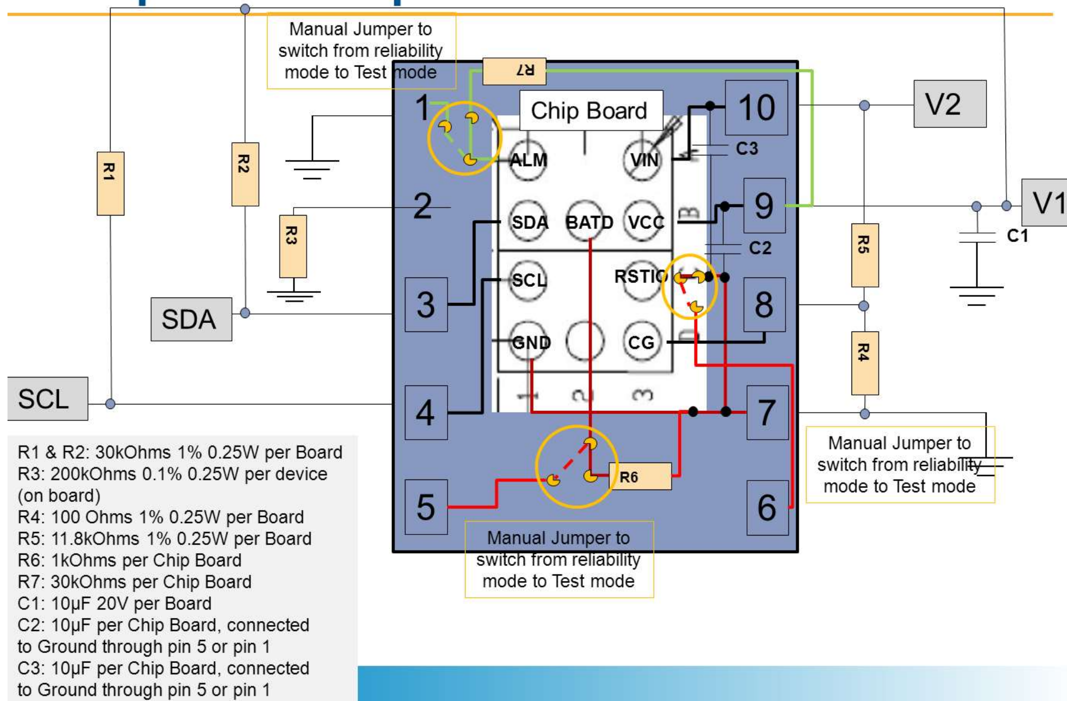
6.3 Test and reliability board Schematics



THB + Chip Board schematic

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6.4 Construction Analysis

GG25LJ WCSP LOT1

Conclusion

CONFORMITY TO QUALIFICATION SUBJECT
CONFORM [X] NOT CONFORM []

- External Analysis
  - Mechanical saw line alignment are within the spec limit as less than 6um
  - Optical and SEM VI observed no major defects except minor side chipping
  - The Package Outline dimension measurement and results to be referred to page 16
  - No void of solder ball seen x-ray analysis
  - The solder bump shear results are in line with spec limit, and failure mode are acceptable as >75% of solder remain.
- X-sectioning and internal analysis
  - Internal VIA, PI, RDL, UBM and PI termination measurement are in the page 26, respectively.

Failure Analysis substeps summary

Substep reference	Step type	Technique	Equipment	Status	Substep completion date	Substep created by	Substep conclusion/comment
SubStep_GNB - AMS_23_00293	Physical Analysis	Solderability	CHEMISTRY;QUAL-77700	SubStep completed	17-FEB-23	BROCHET Xavier	na
SubStep_GNB - AMS_23_00294	Non destructive Inspection	Optical microscopy	KEYENCE VHX7000 - 2	SubStep completed	17-FEB-23	BROCHET Xavier	no defect found

GG25LJ WCSP LOT2

Conclusion

CONFORMITY TO QUALIFICATION SUBJECT
CONFORM [X] NOT CONFORM []

- External Analysis
  - Mechanical saw line alignment are within the spec limit as less than 6um
  - Optical and SEM VI observed no major defects except minor side chipping
  - X-ray analysis shows no solder voids.
  - The Package Outline dimension measurement and results to be referred to page 16

Concern
  - The solder bump shear results are in line with spec limit, failure mode pass with 100% solder residue reaming and no lifted

- X-sectioning and internal analysis
  - Internal VIA, PI, RDL, UBM and PI termination measurement are in the page 26, respectively.
- Overall, no major defect observed.

Failure Analysis substeps summary

Substep reference	Step type	Technique	Equipment	Status	Substep completion date	Substep created by	Substep conclusion/comment
SubStep_GNB - AMS_23_00295	Physical Analysis	Solderability	CHEMISTRY;QUAL-77700	SubStep completed	17-FEB-23	BROCHET Xavier	na
SubStep_GNB - AMS_23_00296	Non destructive Inspection	Optical microscopy	KEYENCE VHX7000 - 2	SubStep completed	17-FEB-23	BROCHET Xavier	no defect found

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GG25LJ WCSP LOT 3

Conclusion

CONFORMITY TO QUALIFICATION SUBJECT
CONFORM [x] NOT CONFORM []

- External Analysis
  - Mechanical saw line alignment are within the spec limit as less than 6um
  - Optical and SEM VI observed no major defects except minor side chipping
  - X-ray analysis shows no solder ball void
  - The Package Outline dimension measurement and results to be referred to page 16

Concern
  - The solder bump shear forces are in line with spec limit, the failure mode shows solder residue remail 100%

- X-sectioning and internal analysis
  - Internal VIA, PI, RDL, UBM and PI termination measurement are in the page 26, respectively.
- Overall, no major defects that deviate the quality was detected.

Failure Analysis substeps summary

Substep reference	Step type	Technique	Equipment	Status	Substep completion date	Substep created by	Substep conclusion/comment
SubStep_GNB - AMS_23_00297	Physical Analysis	Solderability	CHEMISTRY;QUAL-77700	SubStep completed	17-FEB-23	BROCHET Xavier	na
SubStep_GNB - AMS_23_00298	Non destructive Inspection	Optical microscopy	KEYENCE VHX7000 - 1	SubStep completed	17-FEB-23	BROCHET Xavier	no defect found

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Bumping Process Change
PCN Reference : AMS/23/14070

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STC3115AIJT	STC3115IJT	STBB2JAD-R
STBB2J30-R	LD39115J33R	ST1S15J18R

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