Product/Process Change Notice - PCN 23_0142 Rev. -

Analog Devices, Inc. One Analog Way, Wilmington, MA 01887, USA

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title:	Qualification of Alternate Fab Site for eFlash Products
Publication Date:	14-Sep-2023
Effectivity Date:	17-Dec-2023 *(the earliest date that a customer could expect to receive changed material)*
Revision Description:	Initial Release.

Description Of Change:

Analog Devices is adding TSMC Fab 11, USA as an alternate Wafer Fab site to TSMC Fab 3, Taiwan for eFlash products.

Reason For Change:

This change will ensure manufacturing agility and continuity of supply.

Impact of the change (positive or negative) on fit, form, function & reliability:

There is no impact to fit, form, function, or reliability.

Summary of Supporting Information:

Qualification has been performed per AEC-Q100, Stress Test Qualification for Integrated Circuits. See attached Qualification Results Summary.

Supporting Documents

Attachment 1: Type: Delta Qualification Matrix

ADI_PCN_23_0142_Rev_-_PCN-Delta-Qualification-Matrix-ZVEI-5_0_16.xlsm...

Attachment 2: Type: Qualification Results Summary

ADI_PCN_23_0142_Rev_-_Reliability Report.pdf...

Note: If applicable, the device material declaration will be updated due to material change.

ADI Contact Information:

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

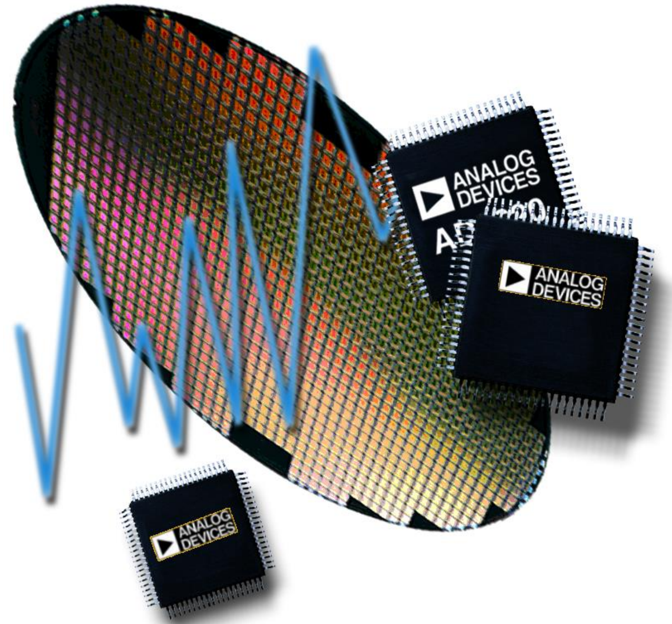
Americas:	Europe:	Japan:	Rest of Asia:
PCN_Americas@analog.com	PCN_Europe@analog.com	PCN_Japan@analog.com	PCN_ROA@analog.com

Appendix A - Affected ADI Models:

Added Parts On This Revision - Product Family / Model Number (3)		
ADUCM330WFS / ADUCM330WFSBCPZ-RL	ADUCM331WFS / ADUCM331WFSBCPZ-RL	ADUCM342 / ADUCM342WFSBCPZ-RL

Appendix B - Revision History:

Rev	Publish Date	Effectivity Date	Rev Description
Rev. -	14-Sep-2023	17-Dec-2023	Initial Release.



Reliability Report

Report Title: eFlash Products at TSMC Fab11 Qualification

Report Number: 20222

Revision: C

Date: 07 September 2023

Summary

This report documents the interim result of the reliability qualification requirements for the release of the eFlash products at TSMC Fab 11.

AECQ100 Qualification Test Methods and Summary

AEC Test Group	AEC Stress Test Name	Abbreviation	AEC Test#	Reference
Group A ACCELERATED ENVIRONMENT STRESS TESTS	Preconditioning	PC	A1	Table 2
	Temperature Humidity Bias or Biased-HAST	THB or HAST	A2	
	Autoclave or Unbiased HAST or Temperature Humidity (without Bias)	AC, UHST, or TH	A3	
	Temperature Cycle	TC	A4	
	Power Temperature Cycling	PTC	A5	
	High Temperature Storage Life	HTSL	A6	
Group B ACCELERATED LIFETIME SIMULATION TESTS	High Temperature Operating Life	HTOL	B1	Table 2
	Early Life Failure Rate	ELFR	B2	
	NVM Endurance, Data Retention, and Operational Life	EDR	B3	
Group C PACKAGE ASSEMBLY INTEGRITY TESTS	Wire Bond Shear	WBS	C1	• Test C2 (and C1 for Cu Wire) are shown in Table 2. • Tests C3-6 are qualified and controlled with inline monitors and may be viewed on-site at Analog Devices.
	Wire Bond Pull Strength	WBP	C2	
	Solderability	SD	C3	
	Physical Dimensions	PD	C4	
	Solder Ball Shear	SBS	C5	
	Lead Integrity	LI	C6	
Group D DIE FABRICATION RELIABILITY TESTS	Electromigration	EM	D1	Die Fabrication Reliability data may be viewed on-site at Analog Devices.
	Time Dependent Dielectric Breakdown	TDDB	D2	
	Hot Carrier Injection	HCI	D3	
	Negative Bias Temperature Instability	BTI	D4	
	Stress Migration	SM	D5	
Group E ELECTRICAL VERIFICATION TESTS	Pre- and Post-Stress Electrical Test	TEST	E1	Table 3 and Table 4
	Electrostatic Discharge Human Body Model	HBM	E2	
	Electrostatic Discharge Charged Device Model	CDM	E3	
	Latch-Up	LU	E4	
	Electrical Distributions	ED	E5	• For Tests E5, E6 and E7, ADI New Product Yield Analysis Testing Guidelines meet AEC-Q100 requirements. • Results for Tests E7-E11 are available as applicable on a case by case basis. • Test E12 results may be viewed on-site at Analog Devices
	Fault Grading	FG	E6	
	Characterization	CHAR	E7	
	Electromagnetic Compatibility	EMC	E9	
	Short Circuit Characterization	SC	E10	
	Soft Error Rate	SER	E11	
	Lead (Pb) Free	LF	E12	
Group F DEFECT SCREENING TESTS	Process Average Test	PAT	F1	ADI New Product Yield Analysis Testing Guidelines meet AEC-Q100 Requirements.
	Statistical Bin/Yield Analysis	SBA	F2	
Group G CAVITY PACKAGE INTEGRITY TESTS	Mechanical Shock	MS	G1	< Applicable only for Cavity-Packages>
	Variable Frequency Vibration	VFV	G2	
	Constant Acceleration	CA	G3	
	Gross/Fine Leak	GFL	G4	
	Package Drop	DROP	G5	
	Lid Torque	LT	G6	
	Die Shear	DS	G7	
	Internal Water Vapor	IWV	G8	

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics

Product Characteristics	Product to be qualified	
Generic/Root Part #	ADUCM342	
Die Id	TMSK07/A	TMJW78/A
Die Size (mm)	3.54 x 3.48	1.56 x 1.81
Wafer Fabrication Site	TSMC Fab11	TSMC Fab8
Wafer Fabrication Process	0.18 µm CMOS Flash	0.18 µm DMOS
Die Substrate	Si	Si
Metallization / # Layers	AlCu(0.5%)/5	AlCu(0.5%)/5
Polyimide	Yes	Yes
Passivation	HDP undoped oxide/Oxide & Nitride	undoped-oxide/SiN

Die/Fab Test Results

Return

Table 2: Reliability Test Results

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
Preconditioning	A1	J-STD-020	MSL-3	ADUCM342	Q20222.1.HO1	0/77	RHC
					Q20222.2.HO2	0/77	RHC
					Q20222.3.HO3	0/77	RHC
HAST[1]	A2	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADUCM341	Q17582.1.HA1	0/77	RH
					Q17582.2.HA2	0/77	RH
					Q17582.3.HA3	0/77	RH
Unbiased HAST[1]	A3	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADUCM341	Q17582.1.UH1	0/77	R
					Q17582.1.UH1	0/77	R
					Q17582.1.UH1	0/77	R
Temperature Cycling (TC)[1]	A4	JESD22-A104	-65°C/+150°C, 1000 Cycles	ADUCM342	Q20222.1.TC1	0/77	RH
					Q20222.2.TC2	0/77	RH
					Q20222.3.TC3	0/77	RH
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 1,000 Hours	ADUCM342	Q20222.1.HS1	0/45	RHC
High Temperature Operating Life (HTOL)[1,2]	B1	JESD22-A108	Ta=125°C<Tj<135°C, Biased, 500 Hours	ADUCM342	Q20222.1.HO1	0/77	RHC
					Q20222.2.HO2	0/77	RHC
					Q20222.3.HO3	0/77	RHC
Early Life Failure Rate (ELFR)	B2	AEC-Q100-008	Ta=125°C<Tj<135°C, Biased, 48 Hours	ADUCM342	Q20222.1.EL1	0/800	RH
					Q20222.2.EL2	0/800	RH
					Q20222.3.EL3	0/800	RH
NVM Endurance, Data Retention[3]	B3	JESD22-A117	Ta=150°C, 500 Hours	ADUCM342	Q20222.1.DRH1	0/77	RH
					Q20222.2.DRH2	0/77	RH
					Q20222.3.DRH3	0/77	RH
NVM Endurance, Data Retention[4]	B3	JESD22-A117	Ta=25°C, 500 Hours	ADUCM342	Q20222.1.DRC1	0/77	R
					Q20222.2.DRC2	0/77	R
					Q20222.3.DRC3	0/77	R
Low Temperature Operating Life (LTOL)[1,5]	-	JESD22-A108	-40°C, Biased, 500 Hours	ADUCM342	Q20222.1.LO1	0/77	RHC
Wire Bond Pull – Post TC	C3	AEC-Q003	3 gF	ADUCM342	Q20222.1.WPT01	0/5	-

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.
[2] These samples were subjected to a 4hrs HTS bake at 180degC followed by 10k Endurance cycling at 115degC prior to HTOL
[3] These samples were subjected to 10k Endurance cycling at 115degC
[4] These samples were subjected to 10k Endurance cycling at 25degC
[5] These samples were subjected to a 4hrs HTS bake at 180degC followed by 10k Endurance cycling at -40degC prior to LTOL

ESD and Latch-Up Test Results

Table 3: ESD Test Result Return

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class	eTest
FICDM	ADUCM342	32-LFCSP	AEC Q100-011	1Ω, Cpkg	±750V (all pins)	C2b	RH
					±1000V (corner pins)	C3	RH
HBM	ADUCM342	32-LFCSP	JS-001	1.5kΩ, 100pF	±4000V	3A	RH

Table 4: Latch Up Test Result Return

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class	eTest
JESD78	ADUCM342	+200mA, -200mA	+4.95V	125°C	II	RH

Approvals:

Reliability Engineer: Roz Rosano