



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/12/7337
Notification Date 06/25/2012

PowerFLAT 5x5 in ECOPACK 2 graded Moulding Compound
Assembly capacity expansion - Carsem (Malaysia)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	18-Jun-2012
Forecasted availability date of samples for customer	18-Jun-2012
Forecasted date for STMicroelectronics change Qualification Plan results availability	18-Jun-2012
Estimated date of changed product first shipment	24-Sep-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly material change
Reason for change	To improve service to Customers by increasing productivity
Description of the change	<p>Following the continuous improvement of our service and in order to rationalize and optimize Power MOSFET Transistors and Power RF productivity, this document is announcing that PowerFLAT 5x5 products, listed in this PCN, will be also produced in Carsem (Malaysia), according to the program to introduce ECOPACK 2 grade products. PowerFLAT 5x5 devices produced in Carsem (Malaysia), guarantee the same quality and electrical characteristics as reported in the relevant data sheets.</p> <p>Devices used for qualification are available as samples</p>
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Will be identified with a letter "G" printed in the ECO Level field
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN IPD-PWR/12/7337
Please sign and return to STMicroelectronics Sales Office		Notification Date 06/25/2012
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark		

DOCUMENT APPROVAL

Name	Function
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Aleo, Mario-Antonio	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager
Petralia, Francesco	Division Q.A. Manager

Dear Customer,

Please be informed that PowerFLAT™ 5x5 Package of Power MOSFET Transistors and Power RF products, manufactured in Carsem (Malaysia) will be also produced, according to the program to introduce ECOPACK 2 grade products.

The involved product series and affected packages are listed in the table below:

Product Family Description	Package	Commercial Product / Series
Power MOSFET Transistors	PowerFLAT™ 5x5	STLxxxxxxx
Power RF		PDxxxxxxx

Any other Product related to the above series, manufactured in PowerFLAT™ 5x5 Package, even if not expressly included or partially mentioned in the attached table, is affected by this change. Some device is not present in the product list because it was created ECOPACK 2 graded moulding compound.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 24-2012.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Description	Part Number - Test Vehicle
Power MOSFET Transistors	STL7NM60N
Power RF	PD54008L-E PD84008L-E

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family Description	1st Shipments
Power MOSFET Transistors Power RF	From Week 37-2012

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipments may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of PowerFLAT™ 5x5 Package, manufactured in Shenzhen (China), Will be identified with a letter “G” printed in the ECO Level field.

Sincerely Yours.



Reliability Report on PowerFLAT™ 5x5 in ECOPACK 2 graded Molding Compound Assembly capacity expansion – Carsem (Malaysia)

General Information		Locations	
Product Lines	M260	Wafer fab	Ang Mo Kio (Singapore)
Product Description	Power MOSFET MDmesh™ II (N-Channel)	Assembly plant	CARSEM (Malaysia)
Commercial Products	STL7NM60N	Reliability Lab	IMS-IPD Catania Reliability Lab
Product Group	IMS – IPD		
Product division	Power Transistor Division		
Package	PowerFLAT™ 5X5 14L		
Silicon Process technology	Power MOSFET (High Voltage)		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	June 2012	7	C. Cappello	G. Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of ECOPACK 2 graded moulding compound PowerFLAT™ 5x5 Package for Power MOSFET Transistors manufactured in Carsem (Malaysia).

3.2 Conclusion

The reliability tests have shown the good performances of the devices toward the environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



4 DEVICE CHARACTERISTICS

4.1 Device description

Power MOSFET MDmesh™ II (N-Channel).

4.2 Construction note

D.U.T.: STL7NM60N LINE: M260 PACKAGE: MLP5x5

Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6" (Singapore)
Technology	Power MOSFET MDmesh™ II (N-Channel)
Die finishing back side	Ti/Ni/Ag
Die size	2410 x 2400 μm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK6" (Singapore)
Test program	WPIS

Assembly information	
Assembly site	CARSEM (Malaysia)
Package description	MLP5x5
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Power Glue
Die attach material	Glue
Wire bonding process	Thermosonic
Wires bonding materials	Au 2 mils Gate Au 2 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	CARSEM (Malaysia)
Tester	TESEC



D.U.T.: STL7NM60N LINE: M260 PACKAGE: MLP5x5

Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6" (Singapore)
Technology	Power MOSFET MDmesh™ II (N-Channel)
Die finishing back side	Ti/Ni/Ag
Die size	2410 x 2400 μm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK6" (Singapore)
Test program	WPIS

Assembly information	
Assembly site	CARSEM (Malaysia)
Package description	MLP5x5
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Power Glue
Die attach material	Glue
Wire bonding process	Thermosonic
Wires bonding materials	Cu 2 mils Gate Cu 2 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	CARSEM (Malaysia)
Tester	TESEC



5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STL7NM60N	M260	Power MOSFET (Au wires)
2	STL7NM60N	M260	Power MOSFET (Cu wires)

5.2 Reliability test plan summary

Lot. 1÷2 - D.U.T.: STL7NM60N LINE: M260 PACKAGE: MLP5x5

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	
						Lot 1	Lot 2
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 260°C 3 times	231 x 2 lots	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning	
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 16V	77 x 2 lots	1000H	0/77	0/77
HTSL	N	JESD22 A-103	Ta = 150°C	77 x 2 lots	1000H	0/77	0/77
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=48V	77 x 2 lots	1000H	0/77	0/77
H3TRB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdd=48V	77 x 2 lots	1000H	0/77	0/77
TC	Y	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77 x 2 lots	500 cy	0/77	0/77
AC	Y	JESD22 A-102	TA=121°C – PA=2 ATM	77 x 2 lots	96 H	0/77	0/77



ANNEXES 6.0

6.1 Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias HTGB High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: <ul style="list-style-type: none">• low power dissipation;• max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.



Reliability Report On ECOPACK 2 graded molding compound in PowerFLAT™ 5x5 Package

TVs: PD54008L-E/PD84008 L-E

General Information		Locations	
Product Line	K24F L560	Wafer fab	CT 6" LIP
Product Description	LDMOS Technology	Assembly plant	CARSEM
P/N	PD54008L-E PD84008 L-E	Reliability Lab	CATANIA Reliability Lab
Product Group	IMS APM - IPC	Reliability assessment	Pass
Product division	Power RF		
Package	PowerFLAT™ 5x5		
Silicon Process technology	LDMOS STH1 LDMOS STH5L		

DOCUMENT INFORMATION

Version	Date	Page s	Prepared by	Approved by	Comment
1.1	12 Dec 2011	7	Alfio Riciputo	Giovanni Presti	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The aim is to qualify the ECOPACK 2 graded molding compound in PowerFLAT™ 5x5 Package for Power MOSFET Transistors manufactured in Carsem (Malaysia).

Shared qualification: PTD and LVR have qualified too the Epoxy Resin in CARSEM HF (sawn QFN).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



4 DEVICE CHARACTERISTICS

4.1 Device description

The devices are common source N-Channel, enhancement-mode lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications.

4.2 Construction note

	K24F - PD54008L-E	L560 - PD84008L-E
Wafer/Die fab. information		
Wafer fab manufacturing location	CT 6" LIP	
Technology	LDMOS	
Process family	LDMOS STH1	LDMOS STH5L
Die finishing back side	Cr/Ni/Au	
Die size	4154x1284 μm^2	4160x1200 μm^2
Bond pad metallization layers	AlSiCu	
Passivation type	Nitride	
Wafer Testing (EWS) information		
Electrical testing manufact. location	CT	
Tester	T84	
Assembly information		
Assembly site	CARSEM	
Package description	PowerFLAT™ 5x5	
Wires bonding materials/diameters	Au/ 1.2mils	
Molding Compound	Epoxy Resin	
Final testing information		
Testing location	CARSEM	
Tester	TESEC	



5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Data Code	Resin	Process/ Package	Product Line	Comments
1	Y107780	127	G770HC	LDMOS STH1 PowerFLAT™ 5x5	K24F	PD54008L-E
2	Y110808			LDMOS STH5 PowerFLAT™ 5x5	L560	PD84008L-E

5.2 Test plan and results summary

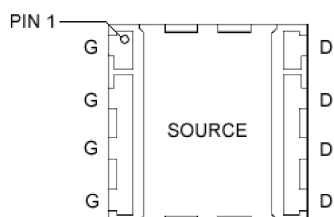
P/N PD54008L-E
P/N PD84008L-E

Test	PC	Std ref.	Conditions		Steps	Failure/SS		Note
						Lot 1	Lot 2	
Die Oriented Tests								
HTFB	N	JESD22 A-108	Tj = 150°C, 15V		168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	
HTRB	N	JESD22 A-108	Tj = 150°C, 20V		168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 175°C		168 H	0/45	0/45	
					500 H	0/45	0/45	
					1000 H	0/45	0/45	
Package Oriented Tests								
PC		JESD22 A-113	Drying 24 H @ 125°C Store 40 H @ Ta=60°C Rh=60% Oven Reflow @ Tpeak=260°C 3times		Final	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	
					200 cy	0/77	0/77	
					500 cy	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, 20V		168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	

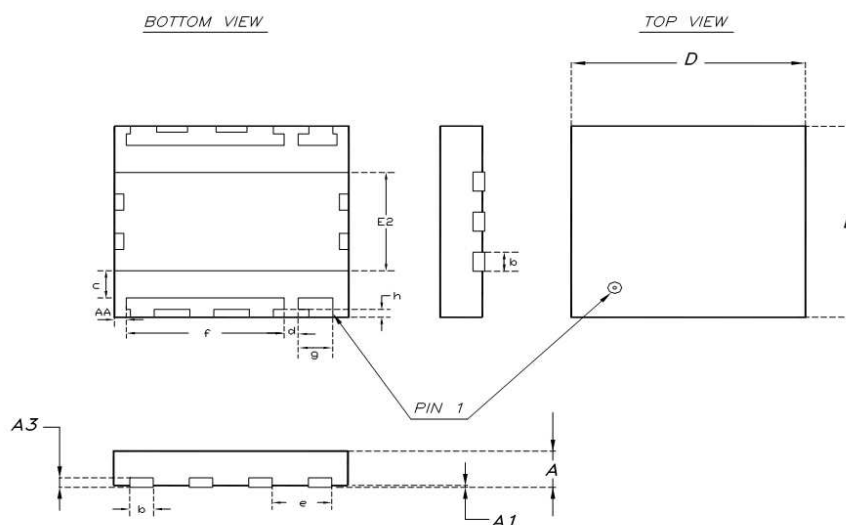
6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Package outline/Mechanical data



Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.24			0.009	
AA	0.15	0.25	0.35	0.006	0.01	0.014
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
d		0.30			0.011	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	
f		3.37			0.132	
g		0.74			0.03	
h		0.21			0.008	



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias HTFB High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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