PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/12/7309
Notification Date 06/12/2012

Front-End Capacity Extension for IGBTs Automotive Ang Mo Kio (Singapore)

Table 1. Change Implementation Schedule

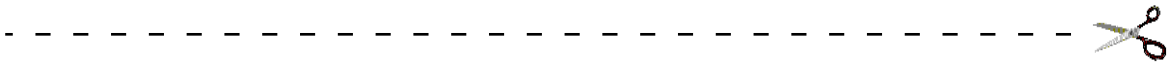
Forecasted implementation date for change	05-Jun-2012
Forecasted availabillity date of samples for customer	05-Jun-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	05-Jun-2012
Estimated date of changed product first shipment	01-Dec-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see taached list
Type of change	Waferfab process change
Reason for change	To be in line with ISO-TS16949
Description of the change	According to the ISO-TS16949 and in order to guarantee a double production source, this document is announcing that IGBTs Automotive grade, currently manufactured in Catania (CT6) Wafer FAB, will be also produced in 6" wafer dimension in the ST's Ang Mo Kio (Singapore) plant. IGBTs Automotive grade, produced in Ang Mo Kio (Singapore), guarantee the same quality and electrical characteristics as reported in the relevant data sheet. Devices used for qualification are available as samples
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	by the digit 6 as front-end code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-PWR/12/7309**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 06/12/2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Division Marketing Manager
Aleo, Mario-Antonio	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

Dear Customer,

According to the ISO-TS16949 and in order to guarantee a double production source, please be informed that IGBTs Automotive grade, currently manufactured in Catania (CT6) Wafer FAB, will be also produced in 6” wafer dimension in the ST’s Ang Mo Kio (Singapore) plant.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 22-2011.

Product Family	Package	Part Number - Test Vehicle
IGBTs	All	STGB10NB40LZT4 STGD18N40LZ-1

Change implementation schedule:

The first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
IGBTs	From Week 48-2012

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of IGBTs Automotive grade, manufactured in 6” wafer dimension in the ST’s Ang Mo Kio (Singapore) plant, will be ensured by the digit 6 as front-end code.

Sincerely Yours.

Reliability Report on Front-End Capacity Extension for AUTOMOTIVE IGBTs Ang Mo Kio (Singapore)

General Information	
Product Lines	LZC5 IZB4
Product Description	IGBT
Commercial Products	STGB10NB40LZT4 STGD18N40LZ-1
Product Group	IMS – IPD
Product division	Power Transistor Division
Package	D^2PAK , DPAK
Silicon Process technology	PT IGBT

Locations	
Wafer fab	*Ang Mo Kio (Singapore)*
Assembly plant	*SHENZHEN (China)*
Reliability Lab	*IMS-IPD Catania Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	May 2012	8	C. Cappello	G. Falcone	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of IGBTs Automotive grade made in 6” wafer dimension in ST`s Ang Mo Kio (Singapore).

3.2 Conclusion

The reliability tests have shown the good performances of the devices toward the environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

IGBTs technology.

4.2 Construction note

D.U.T.: STGB10NB40LZT4 LINE: LZC5 PACKAGE: D^2PAK

Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6" (Singapore)
Technology	PT IGBT
Die finishing back side	Cr/Ni/Au
Die size	4400 x 3570 μm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK6" (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	D^2PAK
Molding compound	Epoxy Resin
Frame material	Selected NiNiP
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Gate Al 10 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP TEST

D.U.T.: STGD18N40LZ-1 LINE: IZB4 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6" (Singapore)
Technology	PT IGBT
Die finishing back side	Cr/Ni/Au
Die size	3990 x 2920 μm^2
Metal	AlSi
Passivation type	Teos + Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK6" (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	DPAK
Molding compound	Epoxy Resin
Frame material	Selected NiNiP
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Gate Al 10 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP TEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STGB10NB40LZT4	LZC5	IGBT
2		LZC5	IGBT
3		LZC5	IGBT
1	STGD18N40LZ-1	IZB4	IGBT
2		IZB4	IGBT
3		IZB4	IGBT

5.2 Reliability test plan summary

Lot. 1÷3 - D.U.T.: STGB10NB40LZT4 LINE: LZC5 PACKAGE: D^2PAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
HTRB	N	JEDD22 A-108	TA = 175℃, Vbias=330V	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTGB	N	JEDD22 A-108	Tj=150℃, Vbias=12V	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTSL	N	JESD22 A-103	TA=175℃	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
PC	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% IR Reflow @ 245℃ 3 times	251 x 3 Lots	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	77 x 3 Lots	96 H	0/77	
TC	Y	JESD22 A-104	TA=-55℃ TO +150℃	77 x 3 Lots	100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	
					1000 cy	0/77	
TF / IOL	Y	Mil-STD 750D Method 1037	ΔTc=+105℃ Pd = 3.8 W	20 x 3 Lots	5K cy	0/20	
					10K cy	0/20	
H3TRB	Y	JESD22 A-101	TA=85℃, RH=85% Vbias=100V	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	

Lot. 1÷3 - D.U.T.: STGD18N40LZ-1 LINE: IZB4 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
HTRB	N	JEDD22 A-108	TA = 175℃, Vbias=290V	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTGB	N	JEDD22 A-108	Tj=150℃, Vbias=20V	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTSL	N	JESD22 A-103	TA=175℃	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
PC	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% IR Reflow @ 260℃ 3 times	251 x 3 Lots	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	77 x 3 Lots	96 H	0/77	
TC	Y	JESD22 A-104	TA=-55℃ TO +150℃	77 x 3 Lots	100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	
					1000 cy	0/77	
TF / IOL	Y	Mil-STD 750D Method 1037	ΔTc=+105℃ Pd = 2 W	20 x 3 Lots	5K cy	0/20	
					10K cy	0/20	
H3TRB	Y	JESD22 A-101	TA=85℃, RH=85% Vbias=100V	77 x 3 Lots	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

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