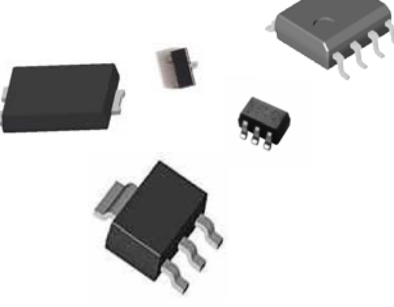
www.diodes.com



Diodes Incorporated for Discrete and Analog Semiconductors

QPAK/PPAP

Qualification Report

Manufacturer No.:	**PCN-2061 – Qualification of "Diodes Technology (Cheng Du) Company Limited" (DTC) as an Additional Assembly & Test Site for SOT-23 Packaged Parts**
Revision	**0**
Date:	**August 19, 2011**
Qualified By:	**Shanghai Kaihong Electronic Co., Ltd. & Diodes Shanghai Co., Ltd.**
Also Applicable To:	**See included PCN notification for affected parts list. All listed parts are Qualified By Similarity (QBS) to the devices for which Reliability Test Summary data is provided within this report.**

Refer to www.diodes.com for data sheets for affected parts.

Prepared By:	**Diodes US Document Control**	**Date**	**August 19, 2011**
Approved By:	**Diodes US QRA Department**	**Date**	**August 19, 2011**

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DIODES INCORPORATED
4949 Hedgcoxe Road, Suite # 200, Plano, TX 75024 USA
www.diodes.com

Quality and Reliability Data Notice

Plastic encapsulated Diodes Incorporated semiconductor devices are not designed and are not warranted to be suitable for use in some military applications and/or military environments. Use of plastic encapsulated Diodes Incorporated semiconductor devices in military applications and/or military environments, in lieu of hermetically sealed ceramic devices, is understood to be fully at the risk of Buyer.

Quality and reliability data provided by Diodes Incorporated is intended to be an estimate of product performance based upon history only. It does not imply that any performance levels reflected in such data can be met if the product is operated outside the conditions expressly stated in the latest published data sheet for a device.

Existing industry standards for plastic encapsulated microcircuit qualification and reliability monitors are based upon historical data, experiments, and field experience with the use of these devices in commercial and industrial applications. The applicability of these standards in determining the suitability for use and safety performance in life support, military and aerospace applications has not been established. Due to the multiple variations in field operating conditions, a component manufacturer can only base estimates of product life on models and the results of package and die level qualification. The buyer's use of this data, and all consequences of such use, is solely the buyer's responsibility. Buyer assumes full responsibility to perform sufficient engineering and additional qualification testing in order to properly evaluate the buyer's application and determine whether a candidate device is suitable for use in that application. The information provided by Diodes Incorporated shall not be considered sufficient grounds on which to base any such determination.

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DIODES INCORPORATED
4949 Hedgcoxe Road, Suite # 200
Plano, TX 75024 USA
(972) 987-3900
www.diodes.com

DATE: 19th August, 2011

PCN #: 2061

PCN Title: Qualification of "Diodes Technology (Cheng Du) Company Limited" (DTC) as an Additional Assembly & Test Site for SOT-23 Packaged Parts

Dear Customer:

This is an announcement of change(s) to products that are currently being offered by Diodes Incorporated.

We request that you acknowledge receipt of this notification within 30 days of the date of this PCN. If you require samples for evaluation purposes, please make a request within 30 days as well. Otherwise, samples may not be built prior to this change. Please refer to the implementation date of this change as it is stated in the attached PCN form. Please contact your local Diodes sales representative to acknowledge receipt of this PCN and for any sample requests.

The changes announced in this PCN will not be implemented earlier than 90 days from the notification date stated in the attached PCN form.

Previously agreed upon customer specific change process requirements or device specific requirements will be addressed separately.

For questions or clarification regarding this PCN, please contact your local Diodes sales representative.

Sincerely,

Diodes Incorporated PCN Team

PRODUCT CHANGE NOTICE PCN-2061 REV 0

Notification Date:	Implementation Date:	Product Family:	Change Type:	PCN #:
19th August, 2011	17th November, 2011	Discrete Semiconductors	Additional Assembly / Test Site	**2061**

TITLE

Qualification of "Diodes Technology (Cheng Du) Company Limited" (DTC) as an Additional Assembly & Test Site for SOT-23 Packaged Parts

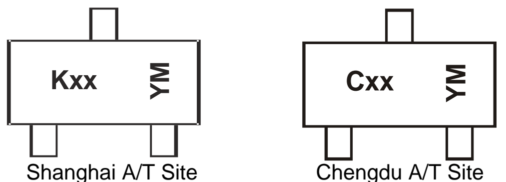
DESCRIPTION OF CHANGE

This PCN is being issued to notify customers that in order to assure continuity of supply, Diodes has qualified "Diodes Technology (Cheng Du) Company Limited" (DTC) located in the Chengdu Hi-Tech Industrial Development Zone (CDHT) in Chengdu, China as an additional Assembly & Test Site for select SOT-23 packaged parts using Copper bond wire.

Established in December 2010, as a joint venture between Diodes Incorporated and Chengdu Ya Guang Electronic Company Limited, Diodes Technology (Chengdu) Company Limited (DTC) was formed to perform semiconductor manufacturing assembly and test functions, and is an expansion of the Company's existing manufacturing presence in Shanghai, China. Ramp to high volume production began in May of 2011.

Full electrical characterization and high reliability testing has been completed on representative part numbers to ensure there is no change to device functionality or electrical specifications in the datasheet.

Part marking will be as follows:



K = SAT (Shanghai Assembly / Test site)
C = CAT (Chengdu Assembly / Test site)
xx = Product Type Marking Code per device data sheet
YM = Date Code Marking
Y = Year (ex: Y = 2011)
M = Month (ex: 8 = August)

IMPACT

Continuity of Supply

PRODUCTS AFFECTED

2N7002-13-F	BAV70-13-F	BC847B-13-F	DMN601K-7	MMBT2907A-7-F
2N7002-7-F	BAV70-7-F	BC847B-7-F	MMBD4148-7-F	MMBT3904-7-F
2N7002A-7	BAV99-13-F	BS870-7-F	MMBD7000-7-F	MMBT3906-7-F
2N7002E-7-F	BAV99-7-F	BSS123-13-F	MMBD914-7-F	MMBT4401-13-F
2N7002K-7	BAW56-13-F	BSS123-7-F	MMBF170-7-F	MMBT4401-7-F
BAL99-7-F	BAW56-7-F	BSS138-7-F	MMBT2222A-13-F	MMBTA05-7-F
BAS16-13-F	BC846B-13-F	BSS84-7-F	MMBT2222A-7-F	MMBTA06-7-F
BAS16-7-F	BC846B-7-F	DMN2004K-7	MMBT2907A-13-F	

WEB LINKS	
Manufacturer's Notice:	http://www.diodes.com/quality/pcns
For More Information Contact:	http://www.diodes.com/contacts
Data Sheet:	http://www.diodes.com/products
DISCLAIMER	
Unless a Diodes Incorporated Sales representative is contacted in writing within 30 days of the posting of this notice, all changes described in this announcement are considered approved.	

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160℃
DIC P/N	2N7002-7-F-31	**Lead material type**	Alloy 42
Package Type	SOT-23	**Lead Material manufacturer**	MHT / SLC
DIE P/N	ON14381	**Lead plating/ coating**	Leadfree
Die line or process	MOSFET	**Lead frame material type**	Alloy 42
Wafer Diameter	8"	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	HHNEC	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Front metal type (Top layer)**	AlCu
Die attach Method / Material	EUTECTIC / NA	**Front metal thickness (Top layer)**	3.5um
Bond wire material & dia.	Tanaka Cu / Heraeus Cu / Pd coated Cu wire, 1.0mil	**Back metal type (All layers)**	Ti/Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	100A/10KA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	Gate *1 + Source *1	**Die size (width x length x thickness) in mm**	0.4*0.4*0.178mm
Package material type	KTMC1050G	**Die passivation thickness range**	PE-SION 10000A
Package material manufacturer	KCC	**No. of mask steps**	7

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Liang Gao	March 10, 2011	Gan Yao	March 15, 2011
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER : 2N7002 SWR110307 Package Description:SOT23		CUSTOMER: DIODES INC.:		
LABORATORY (If Different):		PART DESCRIPTION: Qualification for wafer P/N:ON14381,1.0mil CW,KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic BVDSS@VGS=0V, ID=10uA Characteristic IDSS@VDS=60V, VGS=0V Characteristic IGSS@VGS=±20V, VDS=0V Characteristic VGS(th)@VDS=10V, ID=250uA Characteristic RDSON@VGS=10V, ID=500mA Characteristic RDSON@VGS=5V, ID=50mA Characteristic yFS@VDS=10V,ID=0.2A Characteristic VSD@VGS=0V,ID=0.115A	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vd=48V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vd=48V, PER JESD22 A-108	1	77	0/77	
	@ 1000 Hours	T=150*C Vd=48V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	T=150*C Vg=20V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500Hours	T=150*C Vg=20V, PER JESD22 A-108	1	77	0/77	
	@ 1000 Hours	T=150*C Vg=20V, PER JESD22 A-108	1	77	0/77	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	@ 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	HAST	T=130*C RH=85% Vd=42V	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vd=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vd=1.5V/Id=200mA;PER MIL-STD-750 METHOD 1037	1	77		
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	@ 7500 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	15000cycles@2 mins on/off
	@ 15000 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	pass	MM 50V HBM 100V
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C@30sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS)	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary: The lot passed pre-con and 1000hrs hi-rel tests.						
Submitted by: Michael Yu 6/8/11		**Approved by: Adam Gu 6/8/11**				

Q-Form Q014-4,Rev.K

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160℃
DIC P/N	MMBT3904-7-F-31	**Lead material type**	Alloy 42
Package Type	SOT-23	**Lead Material manufacturer**	MHT / SLC
DIE P/N	C3904E	**Lead plating/ coating**	Leadfree
Die line or process	BJT	**Lead frame material type**	Alloy 42
Wafer Diameter	6"	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case ($θ_{JC}$)**	NA
Assembly Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Max thermal resistance junction to ambient ($θ_{JA}$)***	NA
Test Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Front metal type (Top layer)**	AL
Die attach Method / Material	EUTECTIC / NA	**Front metal thickness (Top layer)**	N/A
Bond wire material & dia.	Tanaka Cu / Heraeus Cu / Pd coated Cu wire, 1.0mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.31*0.40*0.216mm
Package material type	KTMC1050G	**Die passivation thickness range**	Not specified
Package material manufacturer	KCC	**No. of mask steps**	NA

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Liang Gao	March 10, 2011	Gan Yao	March 15, 2011
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: MMBT3904-7-F-31 SWR110306 Package: SOT23			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: KFAB wafer:C3904E,1.0Cu(Tanaka) + KTMC1050G + MHT LDF				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55°C, Ta2=25°C, Ta3=85°C, Ta4=150°C Characteristic BVCBO@IC=10uA, IE=0 Characteristic BVCEO@IC=1.0mA, IB=0 Characteristic BVEBO@IE=10uA, IC=0 Characteristic ICEX@VCE=30V, VEB(OFF)=3.0V Characteristic IBL@VCE=30V, VEB(OFF)=3.0V Characteristic HFE@IC=100uA, VCE=1.0V Characteristic HFE@IC=1.0mA, VCE=1.0V Characteristic HFE@IC=10mA, VCE=1.0V Characteristic HFE@IC=50mA, VCE=1.0V Characteristic HFE@IC=100mA, VCE=1.0V Characteristic VCE(SAT)@IC=10mA, IB=1.0mA Characteristic VCE(SAT)@IC=50mA, IB=5.0mA Characteristic VBE(SAT)@IC=10mA, IB=1.0mA Characteristic VBE(SAT)@IC=50mA, IB=5.0mA	1	25	0/25	
	Lot #2		N/A	N/A		N/A
	Lot #3		N/A	N/A		N/A
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=48V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=48V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150°C Vc=48V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-65°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=48V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85°C RH=85% Vc=48V	1	77	0/77	
	Final 1000 Hours	T=85°C RH=85% Vc=48V	1	77	0/77	
7.3.6.5(10)	HAST	T=130°C RH=85% Vc=42V	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130°C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (11)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (12)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	pass	MM 400V HBM 8kV
7.3.5.10 (13)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		N/A
7.3.5.11 (14)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (15)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (16)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(17)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(18)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(19)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(20)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (21)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260°C@30sec
7.3.5.15 (22)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245°C@5sec
7.3.5.16 (23)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (24)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (25)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (26)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(27)	UNCLAMPED INDUCTIVE SWITCHING (UIS)	N/A, not for Diode	N/A	N/A		N/A
(28)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	This lot passed on 1000hrs hi-rel test.					
Submitted by:	Sean Huang 06/22/11	Approved by: Susan Ding 06/22/11				

*

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160℃
DIC P/N	BAS16-7-F-31	**Lead material type**	Alloy 42
Package Type	SOT-23	**Lead Material manufacturer**	MHT / SLC
DIE P/N	B1001F	**Lead plating/ coating**	Leadfree
Die line or process	Switch	**Lead frame material type**	Alloy 42
Wafer Diameter	6"	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case ($θ_{JC}$)**	NA
Assembly Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Max thermal resistance junction to ambient ($θ_{JA}$)***	NA
Test Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Front metal type (Top layer)**	AL
Die attach Method / Material	EUTECTIC / NA	**Front metal thickness (Top layer)**	N/A
Bond wire material & dia.	Tanaka Cu / Heraeus Cu / Pd coated Cu wire, 1.0mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.28*0.28*0.216mm
Package material type	KTMC1050G	**Die passivation thickness range**	Not specified
Package material manufacturer	KCC	**No. of mask steps**	NA

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Liang Gao	March 10, 2011	GAN YAO	March 15, 2011
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :BAS16 SWR110305 CUSTOMER: Package:SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer B1001F qual;1.0Cu;MHT LDF				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=100uA Characteristic VF@IF=1.0mA Characteristic VF@IF=10mA Characteristic VF@IF=50mA Characteristic VF@IF=150mA Characteristic IR @VR=75V Characteristic IR@VR=20V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C VR=60V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C VR=60V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C VR=60V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9)	HAST	T=130*C RH=85% Vr=42V				
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vr=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	IF=200mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	pass	MM 400V HBM 3kV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 06/05/11		Approved by:Adam Gu 06/05/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160℃
DIC P/N	BAV99-7-F-31	**Lead material type**	Alloy 42
Package Type	SOT-23	**Lead Material manufacturer**	MHT / SLC
DIE P/N	B1001F	**Lead plating/ coating**	Leadfree
Die line or process	Switch	**Lead frame material type**	Alloy 42
Wafer Diameter	6"	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES TECHNOLOGY (CHENGDU) Co., Ltd. Plant 1, No.8 Kexin Road, Chengdu Hi-Tech Zone (West Park), Chengdu, Sichuang, P.R.China 611731	**Front metal type (Top layer)**	AL
Die attach Method / Material	EUTECTIC / NA	**Front metal thickness (Top layer)**	N/A
Bond wire material & dia.	Tanaka Cu / Heraeus Cu / Pd coated Cu wire, 1.0mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.28*0.28*0.216mm
Package material type	KTMC1050G	**Die passivation thickness range**	Not specified
Package material manufacturer	KCC	**No. of mask steps**	NA

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

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Completed by		Date	Certified by	Date
Typed/Printed	Liang Gao	March 10, 2011	Gan Yao	March 15, 2011
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :BAV99 SWR110304 CUSTOMER: Package:SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer B1001F qual;1.0Cu;MHT LDF				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
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	Lot #2		2 of 3	25		
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7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
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(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 06/01/11		Approved by:Adam Gu 06/01/11				