# Data Sheet Revision of the AD9543/AD9545/AD9546 I2C Specification

The proposed changes to the Table 29 in the AD9545 rev C data sheet are emphasized below highlighted in yellow:

Parameter	Min	Тур	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUTS)					Valid for VDDIOA = 1.8 V, 2.5 V, and
Input Logic 1 Voltage	70			% of VDDIOA	3.3 V
Input Logic 0 Voltage			0.3 × VDDIOA	V	
Input Current	-10		+10	μΑ	For $V_{IN} = 10\%$ to 90% of VDDIOA
Hysteresis of Schmitt Trigger Inputs	1.5			% of VDDIOA	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.2	V	$I_{OUT} = 3 \text{ mA}$
Output Fall Time from V <sub>H</sub> Minimum to V <sub>IL</sub> Maximum	20 + 0.1 × C <sub>B</sub>		250	ns	$10 \text{ pF} \leq C_B \leq 400 \text{ pF}$
TIMING					
SCL Clock Rate			400	kHz	
Bus Free Time Between a Stop and Start Condition, t <sub>BUF</sub>	1.3			μs	
Repeated Start Condition Setup Time, t <sub>SU; STA</sub>	0.6			μs	
Repeated Hold Time Start Condition, t <sub>HD; STA</sub>	0.6			μs	After this period, the first clock pulse is generated
Stop Condition Setup Time, t <sub>SU;</sub>	0.6			μs	
STO					
Low Period of the SCL Clock, t <sub>LOW</sub>	1.3			μs	
High Period of the SCL Clock,	0.6			μs	
tнigh					
SCL/SDA Rise Time, t <sub>R</sub>	20 + 0.1 × C <sub>B</sub>		300	ns	
SCL/SDA Fall Time, t⊧	20 + 0.1 × C <sub>B</sub>		300	ns	Min specification requires configuring SDIO/SDA pin for low drive strength (bit 7 in register 0x0109 set to 1)
Data Setup Time, tsu; DAT	100			ns	
Data Hold Time, t <sub>HD; DAT</sub>	100			ns	Not compliant with the I <sup>2</sup> C specification of 0 µs min, 0.9 µs max in fast mode
Capacitive Load for Each Bus Line, C <sub>B</sub>			400	pF	

# Reasons for the proposals:

## t<sub>F</sub>: Fall time of both SDA and SCL signals

The AD9545  $t_f$  range is 20 + 0.1 $C_b$  ns min to 300 ns max, which supports the I2C specification of the same range in fast mode. We measured 18.6 ns fall time when the AD9545 generates ACK, which does not meet the 20+0.1 $C_b$  ns min specification. We saw that lowering the drive strength of the AD9545 SDIO/SDA pin (bit 7 of register 0x109 set to 1) increases the fall time to 54 ns. The customer that found this accepted this approach.

### $t_{\text{R}}\text{:}$ Rise time for both SDA and SCL signals

I looked at the SDA rise time and it was 194ns, well within the data sheet specification range. I do not believe we should modify this specification entry.

SCL being generated by the controller does not make sense to check and specify.

### $t_{\text{HD;DAT}}$ : Data hold time for I2C-bus devices

The AD9545  $t_{HD;DAT}$  min is 100 ns, which does not meet the I2C specification of 0  $\mu$ s min for both standard and fast modes. Also, the I2C specification has 3.45  $\mu$ s max in standard mode and 0.9  $\mu$ s in fast mode. AD9545 does not have any max value specified.