ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. All voltages relative to V_{SS}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Regulator							
$V_{Z(VDD)}$	V_{DD} Shunt Regulator Voltage	I = 1mA	●	~~11.5~~ 11	~~12~~ 11.7	12.5	V
$\Delta V_{Z(VDD)}$	V_{DD} Shunt Regulator Load Regulation	I = 1mA to 5mA ~~LTC4366C/I/H~~	●		30	90	~~mV~~
		~~LTC4366MP~~	●		~~30~~ 60	130	mV
V_{DD}	V_{DD} Supply Voltage (Note 3)		●	4.5		$V_{Z(VDD)}$	V
$I_{VDD(STLO)}$	V_{DD} Pin Current – Start-Up, Gate Low	GATE = 0V, V_{DD} = 7V, OUT = 0V	●		15	23	µA
$I_{VDD(STHI)}$	V_{DD} Pin Current – Start-Up, Gate High	GATE Open, V_{DD} = 7V, OUT = 0V	●		~~9~~ 8	13	µA
$I_{VDD(SD)}$	V_{DD} Pin Current – Shutdown	V_{DD} = 7V, OUT = 0V	●		5	8	µA
OUT Regulator							
$V_{Z(OUT)}$	OUT Shunt Regulator Voltage	I = 1mA, BASE = 0V	●	5.0	~~5.7~~ 5.5	6.0	V
$\Delta V_{Z(OUT)}$	OUT Shunt Regulator Load Regulation	I = 1mA to 5mA	●		30	70	mV
OUT	OUT Supply Voltage (Note 3)		●	3.0		$V_{Z(OUT)}$	V
V_{UVLO1}	OUT Undervoltage Lockout 1	Rising ~~LTC4366C/I/H~~	●	~~2.42~~	~~2.55~~	~~2.75~~	~~V~~
		~~LTC4366MP~~	●	2.42	~~2.55~~ 2.6	2.80	V
ΔV_{UVH1}	OUT Undervoltage Lockout 1 Hysteresis		●	0.2	0.28	0.4	V
V_{UVLO2}	OUT Undervoltage Lockout 2	Rising	●	4.5	4.75	4.9	V
ΔV_{UVH2}	OUT Undervoltage Lockout 2 Hysteresis		●	0.3	0.4	0.5	V
$I_{OUT(AMP)}$	OUT Pin Current – Regulation Amplifier On		●		37	54	µA
$I_{OUT(CP)}$	OUT Pin Current – Charge Pump On		●		150	220	µA
$I_{OUT(SD)}$	OUT Pin Current – Shutdown		●		3	6	µA
BASE, V_{SS}							
$V_{Z(BASE)}$	BASE Shunt Regulator Voltage (OUT – BASE)	I = –10µA, OUT = 4.5V	●	5.5	~~6.2~~ 6.1	6.6	V
$\Delta V_{Z(BASE)}$	BASE Shunt Regulator Load Regulation	I = –10µA to –80µA, OUT = 4.5V	●		125	200	mV
I_{BASE}	BASE Pin Leakage Current	OUT = 4.5V, BASE = –0.5V	●	–0.1	–0.8	–5.5	µA
$I_{VSS(AMP)}$	V_{SS} Pin Current – Regulation Amplifier On		●	–30	–45	–72	µA
$I_{VSS(CP)}$	V_{SS} Pin Current – Charge Pump On		●	–108	–160	–230	µA
$I_{VSS(SD)}$	V_{SS} Pin Current – Shutdown		●		–7	–12	µA
GATE Drive					11.75		
ΔV_{GATE}	External N-Channel Gate Drive (GATE – OUT)	OUT = 4.9V, I = 0, –1µA	●	11.2	~~12~~	12.5	V
$I_{GATE(ST)}$	GATE Pin Current – Start-Up	GATE = OUT = 0V LTC4366C/I/H	●	–4.5	–7.5	–11	µA
		LTC4366MP	●	–3.2	–7.5	–11	µA
$I_{GATE(CP)}$	GATE Pin Current – Charge Pump On	GATE = 5V, OUT = 4.9V	●	–14	–20	–28	µA
$I_{GATE(FD)}$	GATE Pin Current – Fast Discharge	GATE = 10V, OUT = 4.9V	●	122	200	300	mA
$I_{GATE(FLT)}$	GATE Pin Current – Fault	GATE = 10V, OUT = 4.9V	●	~~0.3~~ 0.25	0.7	~~1.2~~ 1.25	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. All voltages relative to V_{SS}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB, $\overline{SD}$, TIMER							
$V_{FB(REG)}$	3% FB pin Regulation Threshold (OUT – FB)		●	1.193	1.23	1.267	V
I_{FB}	FB Pin Leakage Current	OUT – FB = 1.2V	●		0	±1	µA
$V_{\overline{SD}(TH)}$	$\overline{SD}$ Pin Threshold Voltage (V_{DD} – $\overline{SD}$)	Falling	●	1.0	1.5	2.3	V
$V_{\overline{SD}(HYST)}$	$\overline{SD}$ Pin Hysteresis	LTC4366C/I/H	●	147	280	530	mV
		LTC4366MP	●	129	280 260	530	mV
$I_{\overline{SD}}$	$\overline{SD}$ Pin Input Pull-Up Current	V_{DD} – $\overline{SD}$ = 0.7V LTC4366C/I/H	●	–0.7	–1.6	–3.5	µA
		LTC4366MP	●	–0.5	–1.6	–3.5	µA
$V_{TIMER(H)}$	TIMER Pin Threshold	TIMER Rising, V_{DD} = 7V, OUT = $V_{Z(OUT)}$	●	2.6 2.5	2.8 2.7	3.1	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current	TIMER = 1V LTC4366C/I/H	●	–5.1	–9	–13	µA
		LTC4366MP	●	–4	–9	–13	µA
$I_{TIMER(DN)}$	TIMER Pin Pull-Down Current	TIMER = 1V LTC4366C/I/H	●	0.9	1.8	2.8	µA
		LTC4366MP	●	0.7	1.8	2.8	µA
$I_{TIMER(RATIO)}$	TIMER Pin Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	15	20	25	%
AC Characteristics							
$t_{DLY-\overline{SD}}$	$\overline{SD}$ Low to Gate Low Filter Time	Step V_{DD} – $\overline{SD}$ from 0V to 3V	●	420	700	1200	µs
$t_{DLY-FAST}$	FB Low to Gate Low Delay Time	Step OUT – FB from 0V to 1.3V	●	60	150	300	ns
$t_{D(COOL)}$	Cool-Down Timer (Internal)	V_{DD} = $V_{Z(VDD)}$ LTC4366C/I/H	●	5.9	9	16	Seconds
		LTC4366MP	●	5.9	9 10	19	Seconds

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive.

Note 3: Limits on the maximum rating is defined as whichever limit occurs first. An internal clamp limits the GATE pin to a maximum of 12V above source. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$