PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCI No.	ADG/23/13965
1.3 Title of PCI	Packing and labelling change according MSL 1
1.4 Product Category	TCPP01-M12 TCPP03-M20
1.5 Issue date	2023-04-28

2. PCI Team	
2.1 Contact supplier	
2.1.1 Name	NEMETH KRISZTINA
2.1.2 Phone	+49 89460062210
2.1.3 Email	krisztina.nemeth@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Stephane CHAMARD
2.1.2 Marketing Manager	Philippe LEGER
2.1.3 Quality Manager	Jean-Paul REBRASSE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	(Not Defined)	Subcontractors in Malaysia (TCPP01-M12) and China (TCPP03-M20)

4. Description of change		
	Old	New
4.1 Description	Desiccant & dry bag packing (corresponding to MSL 3)	No desiccant and no dry bag (corresponding to MSL 1)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Packing	

5. Reason / motivation for change	
5.1 Motivation	Adjustment between MSL 1 (Moisture Sensitivity Level 1) initial qualification and packing & labelling.
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	MSL 1 on label.

7. Timing / schedule	
7.1 Date of qualification results	2023-04-18
7.2 Intended start of delivery	2023-07-28
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13965 Qualification reports.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-04-28

9. Attachments (additional documentations)
13965 Public product.pdf 13965 PCI TCPP01 TCPP03.pdf 13965 Qualification reports.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	TCPP01-M12	
	TCPP03-M20	

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Reliability Evaluation Report

Qualification of new product TCPP01-M12

General Information	
Product Description	*Protection*
Part Number	*TCPP01-M12*
Product Group	*ADG*
Product division	*DFD*
Package	*FPN 3x3*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST CATANIA ITALY*
Assembly plant	*SUBCONTRACTOR IN MALAYSIA*
Reliability Lab	*ST TOURS FRANCE*

Reliability Assessment

PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
0.1	19/09/2019	8	Aude DROMEL	Julien MICHELON	Preliminary release
1.0	24/09/2019	8	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB/ H3TRB	Thermal Humidity Bias
MSL	Moisture Sensitivity Level

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is the qualification of the new product TCPP01-M12.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

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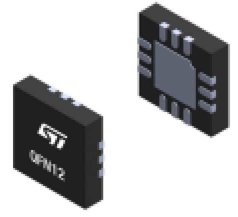
4 DEVICE CHARACTERISTICS

4.1 Device description

TCPP01-M12

Datasheet

USB type-C port protection



Product labels	

Product status link
TCPP01-M12

Product summary	
Order code	TCPP01-M12
Package	QFN12
Packing	Tape and reel
Description	PPS compliant USB type-C port protection

Companion chip	
USB Type-C	STM32 or STM8
USB Type-C with power delivery	STM32 with UCPD support, example STM32L5, STM32G0, STM32G4

Features

- Overvoltage protection on VBUS, adjustable up to 22 V, with external N-channel MOSFET
- 6.0 V overvoltage protection (OVP) on CC lines against short-to-VBUS
- System-level ESD protection for USB type-C connector pins (CC1, CC2), compliant with IEC 61000-4-2 level 4 (±8 kV contact discharge, ±15 kV air discharge)
- Integrated charge pump to control the gate of an external N-channel MOSFET (which features a lower R_{DSON} than a P-channel MOSFET)
- Null quiescent current when no USB charging cable is attached for battery-operated "consumer/sink" applications
- Integrated "dead battery" (R_D resistors)
- Over temperature protection (OTP)
- Operating junction temperature from -40°C to 85°C
- Complies with the latest USB type-C and USB power delivery standards
- Compliant with programmable power supply (PPS) as defined in latest USB PD specification
- Open-drain fault reporting
- ECOPACK2 compliant

Applications

- USB type-C used in sink configuration (consumer)
- USB type-C used in source configuration (provider)
- USB type-C for UFP (upstream facing port) or DFP (downstream facing port) configuration
- USB type-C power delivery, PPS compliant

Description

The TCPP01-M12 (type-C port protection) is a single chip solution for USB type-C port protection that facilitates the migration from USB legacy connectors type-A or type-B to USB type-C connectors. The TCPP01-M12 features 22 V tolerant ESD protection as per IEC61000-4-2 level 4 on USB type-C connector configuration channel (CC) pins. For a safe and reliable USB type-C implementation, the TCPP01-M12 provides overvoltage protection on CC1 and CC2 pins when these pins are subjected to short circuit with the VBUS pin that may happen when removing the USB type-C cable from its receptacle. For sink applications, TCPP01-M12 triggers an external N-MOSFET on VBUS line when a defective power source applies a voltage higher than selected OVP threshold. Also, the TCPP01-M12 integrates a "dead battery" management logic that is compliant with the latest USB power delivery specification. The power supply of the TCPP01-M12 for sink applications operated with a battery can be provided by an MCU 3.3 V GPIO in order to drop the power consumption in "cable not attached" condition down to 0 nA. This low power mode will extend the battery operating life when no source equipment is attached.

The TCPP01-M12 can also be used to protect source (provider) applications, and it can support programmable power supply feature from the USB-C power delivery specification.

4.2 Construction note

	TCPP01-M12
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA ITALY
Technology / Process family	POWER CONTROL PART
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST ANG MO KIO SINGAPORE
Assembly information	
Assembly site	SUBCONTRACTOR - MALAYSIA
Package description	QFN.30.30.09-050-12L-E
Final testing information	
Testing location	SUBCONTRACTOR - MALAYSIA
Comments	

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Die manufacturing plant	Assembly plant	Package	Comments
Lot 1 Lot 2 Lot 3	TCPP01-M12	ST CATANIA	Subcontractor MALAYSIA	FPN 3x3	Qualification lots
Lot 4	MLPQ pitch 500 µm	NA	NA	MLPQ pitch 500 µm	Vehicle test for whiskers
GD1	BBPF-SXM-01Q8Y	ST TOURS	Subcontractor MALAYSIA	FPN 2.8x3	Similar package from same line for solderability tests

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5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.			
						Lot 1	Lot 2	Lot 3	GD1
Die Oriented Tests									
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Temperature=115°C Tension=2V – 3.6V – 20V	77	168h	0/77	-	-	-
					504h	0/77	-	-	-
					1000h	0/77	-	-	-
Package Oriented Tests									
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	77	500cy	-	0/77	-	-
H3TRB/ THB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Tension=2V – 3.6V – 20V	154	168h	-	0/77	0/77	-
					504h	-	0/77	0/77	-
					1000h	-	0/77	0/77	-
Eval MSL1	N	JESD22-A113	Bake + 168h 85°C 85% RH + 3 IR reflows SAM before/after	30	168h	0/30	-	-	-
Solderability	N	JESD22 B-102	Steam Ageing SnAgCu bath 245°C	10	Visual	-	-	-	0/10
			Steam Ageing SnPb 220°C	10	Visual	-	-	-	0/10
			Dry Ageing SnAgCu 245°C	10	Visual	-	-	-	0/10
			Dry Ageing SnPb 220°C	10	Visual	-	-	-	0/10

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.
						Lot 4
Package Oriented Tests						
TC	Y	AEC-Q005	Frequency (cy/h)=2cy/h Temperature (high)=85°C Temperature (low)=-55°C	60	1000cy	0/60
					1500cy	0/60
THS	N		Humidity (HR)=55% Temperature=85°C		6 months	0/60
Room storage	N		Humidity (HR)=60% Temperature=30°C		6 months	0/60

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6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented			
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere..	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB/THB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Whiskers	JESD201A	This test is intended to check Tin plated packages quality versus whiskers risk.	It is applicable for studying tin whisker growth from finishes containing a predominance of tin (Sn).
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.

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Qualification Report

TCPP03-M20

General Information	
Product Line	*Protection*
Product Description	*USB-C protection for dual role power (DRP)*
Product Perimeter	*TCPP03-M20*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*QFN20L 4.0x4.0x0.75mm Package*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST CATANIA – ITALY*
Assembly Plant	*SUBCONTRACTOR – CHINA- (996H)*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	08-September-2021	13	Aude DROMEL	Julien MICHELON	Initial release: TCPP03-M20 qualification

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q005	Pb-Free Test Requirements
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

ESD	Electro-Static Discharge
EV	External Visual
GD	Generic Data
H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
MSL	Moisture Sensitivity Level
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
SD	Solderability test
SS	Sample Size
TC	Temperature Cycling

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify TCPP03-M20 product, USB-C protection for dual role power (DRP) embedded in QFN20L 4.0x4.0x0.75mm package.

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology »

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, MSL search to check the robustness to corrosion and the good package hermeticity.
- Solderability to check compatibility of package with customer assembly.

For some tests, similarity methodology is used. See 5.1 "comments" for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

TCPP03-M20

Datasheet

USB-C protection for dual role power (DRP)

QFN-20L 4.0 x 4.0 x 0.75 mm

Product labels	

Features

- Externally programmable VBUS OVP (over voltage protection) and OCP (over current protection) for provider and consumer power paths with fast turn-off
- Two integrated N-MOSFETs gate drivers for VBUS OVP and OCP
- Very low power in "unattached" state during DRP toggling: 3 µA max. at 125 °C
- Compliant with PPS (programmable power supply) for fast charging, up to 100 W
- Integrated discharge on VBUS and VCONN
- Current sense on VBUS with analog output
- ESD protection for CC1, CC2, compliant with IEC 61000-4-2 Level 4 (±8 kV contact discharge, ±15 kV air discharge)
- V_{CONN} OCP (100 mW max), OVP (6 V max)
- Over voltage protection on CC lines against short-to-V_{BUS}
- Over temperature protection (150 °C typ.)
- Integrated "Dead Battery" management
- I^2C communication, with two I^2C addresses available
- Junction temperature from -40 °C to 125 °C
- Compliant with USB-C power delivery standard 3.1, standard power range (SPR), up to 100 W
- ECOPACK2 compliant

Product status link	
TCPP03-M20	
Order code	TCPP03-M20

Expansion board
X-NUCLEO-DRP1M1

SW expansion for STM32Cube
X-CUBE-TCPP

STM32-UCPD companion chips(1)
STM32G0, STM32G4, STM32L5, STM32U5

1. *Any MCU with USB-C PD SW stack*

I2C address
0110 10x (LSB = 'x')

Applications

- USB type-C power delivery used in dual role power (DRP) or dual role data (DRD) configuration
- USB type-C used in Sink configuration requiring current sense on V_{BUS}
- USB type-C sourcing devices

Description

The TCPP03-M20 is an MCU companion chip enabling cost-effective USB-C power delivery dual role power implementation. It provides protections and functionalities to safely comply with the USB-C Power Delivery specification.

TCPP03-M20 drives external N-MOSFETs on VBUS connector pin in the source and sink power path for over voltage and over current protection. It provides an analog current sense output accessible for an MCU ADC, thus minimizing system cost.

The TCPP03-M20 features 24 V tolerant ESD protection as per IEC61000-4-2 level 4 on USB type-C connector communication channel pins (CC). The TCPP03-M20 provides overvoltage protection on CC1 and CC2 pins when these pins are subjected to short circuit with the VBUS pin that may happen when removing the USB type-C cable from its receptacle.

TCPP03-M20 helps to minimize power consumption during DRP toggling states thanks to its three programmable power modes allowing a power consumption as low as 3 µA maximum, up to 125 °C and thanks to enable pin that wake up the MCU.

4.2 Construction Note

	TCPP03-M20
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA- ITALY
Technology / Process family	POWER CTRL PART
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	SUBCONTRACTOR – CHINA- (996H)
Package description	QFN20L-4.0X4 Package
Molding compound	ECOPACK®2 (“Halogen-free”) molding compound
Lead finishing material	Lead free (pure Tin)
Final testing information	
Testing location	ST TOURS- FRANCE

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

<table>
<tr><th>Lot #</th><th>Part Number</th><th>Package</th><th>Wafer fab location</th><th>Assy plant Location</th><th>Comments</th></tr>
<tr><td>L1</td><td>TCPP03-M20</td><td>QFN20L 4.0X4.0</td><td rowspan="2">ST CATANIA-ITALY-</td><td rowspan="3">SUBCONTRACTOR – CHINA-</td><td>Qualification lot</td></tr>
<tr><td>L2</td><td>TCPP02-M18</td><td>QFN20L-3.5x3.5</td><td>Product with same die technology (different design using same process and plant) in similar package (same Materials, same process, same plant)</td></tr>
<tr><td>GD</td><td>HDMI2C1-4HDS</td><td>QFN20L 4.0X4.0</td><td>ST TOURS</td><td>Similar package (same size, same materials, same process, same plant) for solderability test</td></tr>
</table>

GD: Test vehicles used for similarity.

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020	Lx or GDx	xx	Not applicable for PTH and WLCSP without coating	X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1	30		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1	77	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET - IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	L1	77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET - IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET - IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101			Required for SCR/TRIAC RECTIFIER and Protection devices	
Autoclave	AC	JESD22A-102			Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2	2x77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if ΔTj>100°C cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005	L1	20		X
ESD Characterization	ESD CDM	AEC Q101-001 and 005	Lx or GDx	xx		
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	Lx or GDx	xx	After H3TRB and TC Only for automotive	
Physical Dimension	PD	JESD22B-100	L1	2		X
Terminal Strength	TS	MIL-STD-750 Method 2036	Lx or GDx	xx	Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	Lx or GDx	xx	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	GD	4x10		X
Dead Bug Test	DBT	ST Internal specification	Lx or GDx	xx	Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	Lx or GDx	xx	Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Wire Bond Strength	WBS	MIL-STD-750 Method 2037			Required in case of process change	
Bond Shear	BS	AEC-Q101-003				
Die Shear	DS	MIL-STD-750 Method 2017			Required in case of process change Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET - IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201			Applicable to pure tin plating	
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification			Required for rectifiers and triacs	
Repetitive Surge	RS	Internal specification			Required for protection devices only.	

Low Temperature Storage	LTS	JESD-22 A119: 209	Lx or GDx	xx	AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27	Lx or GDx	xx	AQG324 test for Modules	
Vibration	V	IEC60068-2-6	Lx or GDx	xx	AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS		
						L1	L2	GD
Pre- and Post-Electrical Test		ST datasheet	Ir, Vf,parameters following product datasheet	-	261	0/261		
PC (for SMD packages)		JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	-	154	0/154		
MSL1 research (for SMD packages)	N	JESD22-A113	MSL=1 Reflow=3 Temperature=85°C Humidity (HR)=85%	-	30	0/30		
External Visual		JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process					
Parametric Verification		ST datasheet	Over part temperature range (note 1)		30	Refer to paragraph 6.1 in Annexes		
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=125°C Tension=20V Tension 2=3.3V	1Khrs	77	0/77	-	-
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	77	0/77	-	-
H3TRB (Alt to HAST)	Y	JESD22 A-101	85°C; 85% RH Tension=20V Tension 2=3.3V	1Khrs	77	0/77	0/77	
PD		JESD22 B-100	-	-	2	Refer to paragraph 6.X in Annexes		
SD	N	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-	10			0/10
	N		Dry ageing SnPb bath 220°C	-	10			0/10
	N		Wet ageing SnAgCu bath 245°C	-	10			0/10
	N		Dry ageing SnAgCu bath 245°C	-	10			0/10

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.”

6 ANNEXES

6.1 Parametric Verification

		25°C				Data sheet		
Item	**Unit**	Min.	Mean.	Max	Std Dev.	Min.	Typ.	Max
VBUS_UVLO	V	2.3	2.34	2.4	0.050262	1.9	2.34	2.9
IL_VBUS	mA	0.3825	0.390675	0.3976	0.003412	0.2	0.390675	0.7
VGS	V	5.2721	5.301865	5.3187	0.013006	4.5	5.301865	5.5
IL_VBUS	mA	1.301	1.321	1.356	0.01457	0.5	1.321	2
VGS	V	5.2369	5.267095	5.2834	0.013162	4.5	5.267095	5.5
VOVP_TH	V	1.16	1.1675	1.18	0.005501	1.1	1.1675	1.25
DB_volt1	V	0.9331	0.95088	0.9763	0.009817	0.7	0.95088	1.25
DB_volt2	V	0.9359	0.95024	0.9757	0.009737	0.7	0.95024	1.25
RDB	KOhms	4.7823	4.81923	4.8663	0.021573	4.1	4.81923	5.6
RDB	KOhms	4.7984	4.828265	4.877	0.024899	4.1	4.828265	5.6
RONCC	Ohms	16.4563	16.59255	16.7534	0.061113	8	16.59255	28
RONCC	Ohms	16.8523	16.96765	17.1049	0.070055	8	16.96765	28
I_enable	uA	1.632	1.686	1.8159	0.049193	0	1.686	3
I_enable	uA	2.5655	2.619695	2.6643	0.031532	0	2.619695	10
ICC_VCONN	uA	0.1362	0.151585	0.1699	0.009929	0	0.151585	1
ICC_VCONN	uA	2254.528	2281.186	2307.093	14.24249	0	2281.186	2700
RONCC	Ohms	0.5806	0.636305	0.6958	0.033421	0	0.636305	1.5
RONCC	Ohms	0.6436	0.68104	0.7189	0.020797	0	0.68104	1.5
VTH_CC	V	5.8	5.8395	5.87	0.018202	5.5	5.8395	6
VTH_CC	V	5.75	5.8045	5.85	0.034561	5.5	5.8045	6
RON_VCONN	Ohms	2.9065	2.947525	2.986	0.021136	2.1	2.947525	5.5
OCP_TH_VCONN	mA	48	49.15	50	0.48936	40	49.15	55
RON_VCONN	Ohms	3.039	3.07025	3.0907	0.012983	2.1	3.07025	5.5
VCONN_DIS_RES	KOhms	3.9022	3.9512	4.0099	0.028833	2.5	3.9512	5
VBUS_DIS_res	mA	2.012	2.06313	2.1377	0.033593	1.3	2.06313	3
GDP_VGS_5V	V	5.2403	5.27428	5.2995	0.015448	4.5	5.27428	5.5
IANA_GAIN	V/V	40.6548	41.85838	42.7584	0.519638	39	41.85838	45
VTH_OCP_VBUS	mV	39.2523	40.64515	42.8357	0.822759	35	40.64515	45
TPD_OVP_ON_VBUS	ns	90.2365	95.3245	100.2546	3.02154	0	95.3245	145
TON	ms	0.4125	0.454	0.482	0.0354	0	0.454	3
T_OVP_CC	ns	44.6131	56.28751	70.4513	6.721328	0	56.28751	100
T_OVP_CC	ns	46.15	70.70769	85.5652	12.25706	0	70.70769	100
T_OCP_VCONN	ns	879.0808	912.9525	958.9403	21.14183	0	912.9525	2000
TOFF_OCP_VBUS	us	2.61	2.752	2.85	0.096021	0	2.752	8

6.2 Physical Dimensions

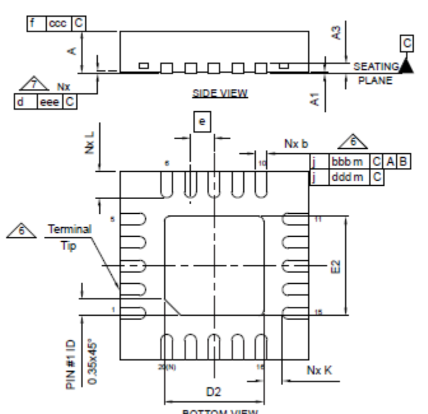

Table 24. QFN-20L 4.0 x 4.0 x 0.75 mm package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1		0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	3.95	4.00	4.05
D2	1.95	2.10	2.20
E	3.95	4.00	4.05
E2	1.95	2.10	2.20
e	0.50 BSC		
L	0.50	0.55	0.60
K	0.20		

DIMENSION	A	b	D	D2	E	E2	L
Data book **Min** (mm)	**0.70**	**0.18**	**3.95**	**1.95**	**3.95**	**1.95**	**0.50**
Data book **Typ** (mm)	**0.75**	**0.25**	**4.00**	**2.10**	**4.00**	**2.10**	**0.55**
Data book **Max** (mm)	**0.80**	**0.30**	**4.05**	**2.20**	**4.05**	**2.20**	**0.60**
1	0.75	0.258	4.015	2.107	4.023	2.122	0.551
2	0.746	0.259	4.015	2.108	4.023	2.117	0.556
3	0.754	0.258	4.016	2.107	4.022	2.118	0.549
4	0.742	0.257	4.018	2.107	4.021	2.122	0.549
5	0.752	0.255	4.016	2.107	4.02	2.119	0.548
6	0.754	0.26	4.017	2.105	4.02	2.119	0.546
7	0.751	0.258	4.017	2.108	4.02	2.118	0.561
8	0.748	0.258	4.018	2.109	4.021	2.12	0.544
9	0.759	0.256	4.016	2.108	4.02	2.123	0.548
10	0.756	0.257	4.017	2.109	4.023	2.12	0.548
11	0.744	0.257	4.018	2.107	4.02	2.119	0.548
12	0.753	0.256	4.017	2.105	4.021	2.123	0.547
13	0.747	0.254	4.018	2.107	4.019	2.121	0.548
14	0.751	0.258	4.016	2.108	4.019	2.121	0.546
15	0.752	0.258	4.018	2.109	4.02	2.118	0.554
16	0.749	0.258	4.019	2.106	4.021	2.12	0.545
17	0.759	0.258	4.018	2.105	4.023	2.122	0.545
18	0.747	0.258	4.018	2.105	4.02	2.12	0.545
19	0.751	0.259	4.017	2.104	4.02	2.123	0.551
20	0.756	0.258	4.016	2.105	4.022	2.121	0.551
MOY	**0.751**	**0.258**	**4.017**	**2.107**	**4.021**	**2.120**	**0.549**
MIN	**0.742**	**0.254**	**4.015**	**2.104**	**4.019**	**2.117**	**0.544**
MAX	**0.759**	**0.260**	**4.019**	**2.109**	**4.023**	**2.123**	**0.561**

6.3 Tests description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
SD Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCI Title : Packing and labelling change according MSL 1

PCI Reference : ADG/23/13965

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TCPP01-M12	TCPP03-M20	

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(1) ADG: Automotive & Discrete Group

PCI
Product/Process Change Information

Packing and labelling change according to

Moisture Sensitivity Level 1 (MSL 1) for TCPP01-M12 & TCPP03-M20

Notification number:	ADG/23/13965	**Issue Date**	26-Apr-2023
Issued by	Isabelle BALLON		
Product series affected by the change		TCPP01-M12 TCPP03-M20	

Reason for change

Codification adjustment in compliance to initial qualification in MSL 1.
Refer to Initial qualification reports (19095QRP & 21058QRP) attached at the end of this document.

Effects of change

Labelling change with MSL 1 indication for TCPP01-M12 and TCPP03-M20.

As Packing is linked to both Moisture Sensitivity Level and Lead finishing material (Second Level Interconnect), packing mode is also adjusted. Refer to details below.

- Packing change for TCPP01-M12 (Second Level Interconnect e3): no Dry packing (no desiccant, no Humidity Indicator Card and no Moisture Barrier Bag).
- Packing change for TCPP03-M20 (Second Level Interconnect e4): Dry packing (1 desiccant + Moisture Barrier Bag sealed under vacuum).

Note: The Pb-free category symbol for the 2nd level interconnect material/finish marked on the manufactured device identifies the 2nd level interconnect material type/finish as specified in JEDEC Standard JESD97:
e3: Sn
e4: NiAu or NiPdAu

Refer to labels and packing photos here after.

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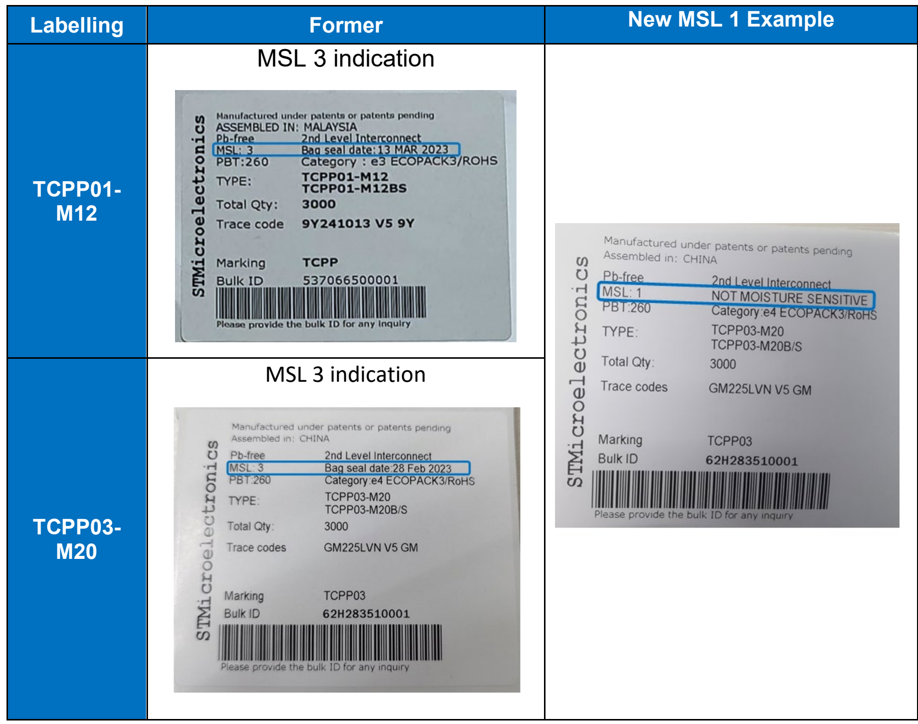

Labelling	Former	New MSL 1 Example
TCPP01-M12	MSL 3 indication	
TCPP03-M20	MSL 3 indication	

Packing	Former	New
TCPP01-M12	**MSL 3 packing** Tape & Reel + Dry packing (desiccants + Humidity Indicator Card + Moisture Barrier Bag sealed under vacuum) = > Pizza box Paste label on reel → Put 1 HIC and 2 desiccant → Paste label on MBB and vacuum seal. → Paste label on box. Seal box with ST seal tape.	**MSL 1 packing (for e3 products)** Tape & Reel => Pizza Box ST label, Test id label: Paste label on reel FG label, ST label: Paste label on box and put reel inside pizza box. ST seal tape: Seal box with QA tape
TCPP03-M20	**MSL 3 packing** Tape & Reel + Dry packing (desiccant + Humidity Indicator Card + Moisture Barrier Bag sealed under vacuum) = > Pizza box	**MSL 1 packing with Dry-packing (for e4 products)** Tape & Reel + Dry packing (desiccant + Moisture Barrier Bag sealed under vacuum) = > Pizza box

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Product identification and traceability

- Traceability on label (indication “MSL: 1 NOT MOISTURE SENSITIVE”).

Qualification complete date	18-April-2023

Change implementation schedule

Sales-types	Estimated production start	Estimated first shipments
TCPP01-M12	**Week 29-2023**	**Week 30-2023**
TCPP03-M20	**Week 29-2023**	**Week 30-2023**

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Reliability Evaluation Report

Qualification of new product TCPP01-M12

General Information	
Product Description	*Protection*
Part Number	*TCPP01-M12*
Product Group	*ADG*
Product division	*DFD*
Package	*FPN 3x3*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST CATANIA ITALY*
Assembly plant	*SUBCONTRACTOR IN MALAYSIA*
Reliability Lab	*ST TOURS FRANCE*

Reliability Assessment

PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
0.1	19/09/2019	8	Aude DROMEL	Julien MICHELON	Preliminary release
1.0	24/09/2019	8	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB/ H3TRB	Thermal Humidity Bias
MSL	Moisture Sensitivity Level

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is the qualification of the new product TCPP01-M12.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

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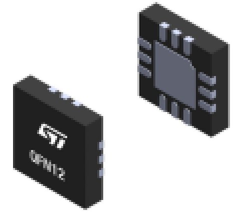
4 DEVICE CHARACTERISTICS

4.1 Device description

TCPP01-M12

Datasheet

USB type-C port protection



Product labels	

Product status link
TCPP01-M12

Product summary	
Order code	TCPP01-M12
Package	QFN12
Packing	Tape and reel
Description	PPS compliant USB type-C port protection

Companion chip	
USB Type-C	STM32 or STM8
USB Type-C with power delivery	STM32 with UCPD support, example STM32L5, STM32G0, STM32G4

Features

- Overvoltage protection on VBUS, adjustable up to 22 V, with external N-channel MOSFET
- 6.0 V overvoltage protection (OVP) on CC lines against short-to-VBUS
- System-level ESD protection for USB type-C connector pins (CC1, CC2), compliant with IEC 61000-4-2 level 4 (±8 kV contact discharge, ±15 kV air discharge)
- Integrated charge pump to control the gate of an external N-channel MOSFET (which features a lower R_{DSON} than a P-channel MOSFET)
- Null quiescent current when no USB charging cable is attached for battery-operated "consumer/sink" applications
- Integrated "dead battery" (R_D resistors)
- Over temperature protection (OTP)
- Operating junction temperature from -40°C to 85°C
- Complies with the latest USB type-C and USB power delivery standards
- Compliant with programmable power supply (PPS) as defined in latest USB PD specification
- Open-drain fault reporting
- ECOPACK2 compliant

Applications

- USB type-C used in sink configuration (consumer)
- USB type-C used in source configuration (provider)
- USB type-C for UFP (upstream facing port) or DFP (downstream facing port) configuration
- USB type-C power delivery, PPS compliant

Description

The TCPP01-M12 (type-C port protection) is a single chip solution for USB type-C port protection that facilitates the migration from USB legacy connectors type-A or type-B to USB type-C connectors. The TCPP01-M12 features 22 V tolerant ESD protection as per IEC61000-4-2 level 4 on USB type-C connector configuration channel (CC) pins. For a safe and reliable USB type-C implementation, the TCPP01-M12 provides overvoltage protection on CC1 and CC2 pins when these pins are subjected to short circuit with the VBUS pin that may happen when removing the USB type-C cable from its receptacle. For sink applications, TCPP01-M12 triggers an external N-MOSFET on VBUS line when a defective power source applies a voltage higher than selected OVP threshold. Also, the TCPP01-M12 integrates a "dead battery" management logic that is compliant with the latest USB power delivery specification. The power supply of the TCPP01-M12 for sink applications operated with a battery can be provided by an MCU 3.3 V GPIO in order to drop the power consumption in "cable not attached" condition down to 0 nA. This low power mode will extend the battery operating life when no source equipment is attached.

The TCPP01-M12 can also be used to protect source (provider) applications, and it can support programmable power supply feature from the USB-C power delivery specification.

4.2 Construction note

	TCPP01-M12
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA ITALY
Technology / Process family	POWER CONTROL PART
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST ANG MO KIO SINGAPORE
Assembly information	
Assembly site	SUBCONTRACTOR - MALAYSIA
Package description	QFN.30.30.09-050-12L-E
Final testing information	
Testing location	SUBCONTRACTOR - MALAYSIA
Comments	

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Die manufacturing plant	Assembly plant	Package	Comments
Lot 1 Lot 2 Lot 3	TCPP01-M12	ST CATANIA	Subcontractor MALAYSIA	FPN 3x3	Qualification lots
Lot 4	MLPQ pitch 500 µm	NA	NA	MLPQ pitch 500 µm	Vehicle test for whiskers
GD1	BBPF-SXM-01Q8Y	ST TOURS	Subcontractor MALAYSIA	FPN 2.8x3	Similar package from same line for solderability tests

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5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.			
						Lot 1	Lot 2	Lot 3	GD1
Die Oriented Tests									
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Temperature=115°C Tension=2V – 3.6V – 20V	77	168h	0/77	-	-	-
					504h	0/77	-	-	-
					1000h	0/77	-	-	-
Package Oriented Tests									
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	77	500cy	-	0/77	-	-
H3TRB/ THB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Tension=2V – 3.6V – 20V	154	168h	-	0/77	0/77	-
					504h	-	0/77	0/77	-
					1000h	-	0/77	0/77	-
Eval MSL1	N	JESD22-A113	Bake + 168h 85°C 85% RH + 3 IR reflows SAM before/after	30	168h	0/30	-	-	-
Solderability	N	JESD22 B-102	Steam Ageing SnAgCu bath 245°C	10	Visual	-	-	-	0/10
			Steam Ageing SnPb 220°C	10	Visual	-	-	-	0/10
			Dry Ageing SnAgCu 245°C	10	Visual	-	-	-	0/10
			Dry Ageing SnPb 220°C	10	Visual	-	-	-	0/10

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.
						Lot 4
Package Oriented Tests						
TC	Y	AEC-Q005	Frequency (cy/h)=2cy/h Temperature (high)=85°C Temperature (low)=-55°C	60	1000cy	0/60
					1500cy	0/60
THS	N		Humidity (HR)=55% Temperature=85°C		6 months	0/60
Room storage	N		Humidity (HR)=60% Temperature=30°C		6 months	0/60

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6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
		Die Oriented	
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
		Package Oriented	
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere..	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB/THB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Whiskers	JESD201A	This test is intended to check Tin plated packages quality versus whiskers risk.	It is applicable for studying tin whisker growth from finishes containing a predominance of tin (Sn).
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.

ST Restricted

Qualification Report

TCPP03-M20

General Information	
Product Line	*Protection*
Product Description	*USB-C protection for dual role power (DRP)*
Product Perimeter	*TCPP03-M20*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*QFN20L 4.0x4.0x0.75mm Package*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST CATANIA – ITALY*
Assembly Plant	*SUBCONTRACTOR – CHINA- (996H)*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	08-September-2021	13	Aude DROMEL	Julien MICHELON	Initial release: TCPP03-M20 qualification

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q005	Pb-Free Test Requirements
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

ESD	Electro-Static Discharge
EV	External Visual
GD	Generic Data
H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
MSL	Moisture Sensitivity Level
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
SD	Solderability test
SS	Sample Size
TC	Temperature Cycling

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify TCPP03-M20 product, USB-C protection for dual role power (DRP) embedded in QFN20L 4.0x4.0x0.75mm package.

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology »

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, MSL search to check the robustness to corrosion and the good package hermeticity.
- Solderability to check compatibility of package with customer assembly.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

TCPP03-M20

Datasheet

USB-C protection for dual role power (DRP)

QFN-20L 4.0 x 4.0 x 0.75 mm

Product labels	

Features

- Externally programmable VBUS OVP (over voltage protection) and OCP (over current protection) for provider and consumer power paths with fast turn-off
- Two integrated N-MOSFETs gate drivers for VBUS OVP and OCP
- Very low power in "unattached" state during DRP toggling: 3 µA max. at 125 °C
- Compliant with PPS (programmable power supply) for fast charging, up to 100 W
- Integrated discharge on VBUS and VCONN
- Current sense on VBUS with analog output
- ESD protection for CC1, CC2, compliant with IEC 61000-4-2 Level 4 (±8 kV contact discharge, ±15 kV air discharge)
- V_{CONN} OCP (100 mW max), OVP (6 V max)
- Over voltage protection on CC lines against short-to-V_{BUS}
- Over temperature protection (150 °C typ.)
- Integrated "Dead Battery" management
- I^2C communication, with two I^2C addresses available
- Junction temperature from -40 °C to 125 °C
- Compliant with USB-C power delivery standard 3.1, standard power range (SPR), up to 100 W
- ECOPACK2 compliant

Product status link	
TCPP03-M20	
Order code	TCPP03-M20

Expansion board
X-NUCLEO-DRP1M1

SW expansion for STM32Cube
X-CUBE-TCPP

STM32-UCPD companion chips(1)
STM32G0, STM32G4, STM32L5, STM32U5

1. *Any MCU with USB-C PD SW stack*

I2C address
0110 10x (LSB = 'x')

Applications

- USB type-C power delivery used in dual role power (DRP) or dual role data (DRD) configuration
- USB type-C used in Sink configuration requiring current sense on V_{BUS}
- USB type-C sourcing devices

Description

The TCPP03-M20 is an MCU companion chip enabling cost-effective USB-C power delivery dual role power implementation. It provides protections and functionalities to safely comply with the USB-C Power Delivery specification.

TCPP03-M20 drives external N-MOSFETs on VBUS connector pin in the source and sink power path for over voltage and over current protection. It provides an analog current sense output accessible for an MCU ADC, thus minimizing system cost.

The TCPP03-M20 features 24 V tolerant ESD protection as per IEC61000-4-2 level 4 on USB type-C connector communication channel pins (CC). The TCPP03-M20 provides overvoltage protection on CC1 and CC2 pins when these pins are subjected to short circuit with the VBUS pin that may happen when removing the USB type-C cable from its receptacle.

TCPP03-M20 helps to minimize power consumption during DRP toggling states thanks to its three programmable power modes allowing a power consumption as low as 3 µA maximum, up to 125 °C and thanks to enable pin that wake up the MCU.

4.2 Construction Note

	TCPP03-M20
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA- ITALY
Technology / Process family	POWER CTRL PART
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	SUBCONTRACTOR – CHINA- (996H)
Package description	QFN20L-4.0X4 Package
Molding compound	ECOPACK®2 (“Halogen-free”) molding compound
Lead finishing material	Lead free (pure Tin)
Final testing information	
Testing location	ST TOURS- FRANCE

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Wafer fab location	Assy plant Location	Comments
L1	TCPP03-M20	QFN20L 4.0X4.0	ST CATANIA- ITALY-	SUBCONTRACTOR – CHINA-	Qualification lot
L2	TCPP02-M18	QFN20L-3.5x3.5			Product with same die technology (different design using same process and plant) in similar package (same Materials, same process, same plant)
GD	HDMI2C1-4HDS	QFN20L 4.0X4.0	ST TOURS		Similar package (same size, same materials, same process, same plant) for solderability test

GD: Test vehicles used for similarity.

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020	Lx or GDx	xx	Not applicable for PTH and WLCSP without coating	X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1	30		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1	77	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET - IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	L1	77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET - IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET - IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101			Required for SCR/TRIAC RECTIFIER and Protection devices	
Autoclave	AC	JESD22A-102			Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2	2x77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if ΔTj>100°C cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005	L1	20		X
ESD Characterization	ESD CDM	AEC Q101-001 and 005	Lx or GDx	xx		
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	Lx or GDx	xx	After H3TRB and TC Only for automotive	
Physical Dimension	PD	JESD22B-100	L1	2		X
Terminal Strength	TS	MIL-STD-750 Method 2036	Lx or GDx	xx	Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	Lx or GDx	xx	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	GD	4x10		X
Dead Bug Test	DBT	ST Internal specification	Lx or GDx	xx	Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	Lx or GDx	xx	Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Wire Bond Strength	WBS	MIL-STD-750 Method 2037			Required in case of process change	
Bond Shear	BS	AEC-Q101-003				
Die Shear	DS	MIL-STD-750 Method 2017			Required in case of process change Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201			Applicable to pure tin plating	
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,…)	FT	Internal specification			Required for rectifiers and triacs	
Repetitive Surge	RS	Internal specification			Required for protection devices only.	

Low Temperature Storage	LTS	JESD-22 A119: 209	Lx or GDx	xx	AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27	Lx or GDx	xx	AQG324 test for Modules	
Vibration	V	IEC60068-2-6	Lx or GDx	xx	AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS		
						L1	L2	GD
Pre- and Post-Electrical Test		ST datasheet	Ir, Vf,parameters following product datasheet	-	261	0/261		
PC (for SMD packages)		JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	-	154	0/154		
MSL1 research (for SMD packages)	N	JESD22-A113	MSL=1 Reflow=3 Temperature=85°C Humidity (HR)=85%	-	30	0/30		
External Visual		JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process					
Parametric Verification		ST datasheet	Over part temperature range (note 1)		30	Refer to paragraph 6.1 in Annexes		
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=125°C Tension=20V Tension 2=3.3V	1Khrs	77	0/77	-	-
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	77	0/77	-	-
H3TRB (Alt to HAST)	Y	JESD22 A-101	85°C; 85% RH Tension=20V Tension 2=3.3V	1Khrs	77	0/77	0/77	
PD		JESD22 B-100	-	-	2	Refer to paragraph 6.X in Annexes		
SD	N	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-	10			0/10
	N		Dry ageing SnPb bath 220°C	-	10			0/10
	N		Wet ageing SnAgCu bath 245°C	-	10			0/10
	N		Dry ageing SnAgCu bath 245°C	-	10			0/10

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.”

6 ANNEXES

6.1 Parametric Verification

		25°C				Data sheet		
Item	**Unit**	Min.	Mean.	Max	Std Dev.	Min.	Typ.	Max
VBUS_UVLO	V	2.3	2.34	2.4	0.050262	1.9	2.34	2.9
IL_VBUS	mA	0.3825	0.390675	0.3976	0.003412	0.2	0.390675	0.7
VGS	V	5.2721	5.301865	5.3187	0.013006	4.5	5.301865	5.5
IL_VBUS	mA	1.301	1.321	1.356	0.01457	0.5	1.321	2
VGS	V	5.2369	5.267095	5.2834	0.013162	4.5	5.267095	5.5
VOVP_TH	V	1.16	1.1675	1.18	0.005501	1.1	1.1675	1.25
DB_volt1	V	0.9331	0.95088	0.9763	0.009817	0.7	0.95088	1.25
DB_volt2	V	0.9359	0.95024	0.9757	0.009737	0.7	0.95024	1.25
RDB	KOhms	4.7823	4.81923	4.8663	0.021573	4.1	4.81923	5.6
RDB	KOhms	4.7984	4.828265	4.877	0.024899	4.1	4.828265	5.6
RONCC	Ohms	16.4563	16.59255	16.7534	0.061113	8	16.59255	28
RONCC	Ohms	16.8523	16.96765	17.1049	0.070055	8	16.96765	28
I_enable	uA	1.632	1.686	1.8159	0.049193	0	1.686	3
I_enable	uA	2.5655	2.619695	2.6643	0.031532	0	2.619695	10
ICC_VCONN	uA	0.1362	0.151585	0.1699	0.009929	0	0.151585	1
ICC_VCONN	uA	2254.528	2281.186	2307.093	14.24249	0	2281.186	2700
RONCC	Ohms	0.5806	0.636305	0.6958	0.033421	0	0.636305	1.5
RONCC	Ohms	0.6436	0.68104	0.7189	0.020797	0	0.68104	1.5
VTH_CC	V	5.8	5.8395	5.87	0.018202	5.5	5.8395	6
VTH_CC	V	5.75	5.8045	5.85	0.034561	5.5	5.8045	6
RON_VCONN	Ohms	2.9065	2.947525	2.986	0.021136	2.1	2.947525	5.5
OCP_TH_VCONN	mA	48	49.15	50	0.48936	40	49.15	55
RON_VCONN	Ohms	3.039	3.07025	3.0907	0.012983	2.1	3.07025	5.5
VCONN_DIS_RES	KOhms	3.9022	3.9512	4.0099	0.028833	2.5	3.9512	5
VBUS_DIS_res	mA	2.012	2.06313	2.1377	0.033593	1.3	2.06313	3
GDP_VGS_5V	V	5.2403	5.27428	5.2995	0.015448	4.5	5.27428	5.5
IANA_GAIN	V/V	40.6548	41.85838	42.7584	0.519638	39	41.85838	45
VTH_OCP_VBUS	mV	39.2523	40.64515	42.8357	0.822759	35	40.64515	45
TPD_OVP_ON_VBUS	ns	90.2365	95.3245	100.2546	3.02154	0	95.3245	145
TON	ms	0.4125	0.454	0.482	0.0354	0	0.454	3
T_OVP_CC	ns	44.6131	56.28751	70.4513	6.721328	0	56.28751	100
T_OVP_CC	ns	46.15	70.70769	85.5652	12.25706	0	70.70769	100
T_OCP_VCONN	ns	879.0808	912.9525	958.9403	21.14183	0	912.9525	2000
TOFF_OCP_VBUS	us	2.61	2.752	2.85	0.096021	0	2.752	8

6.2 Physical Dimensions

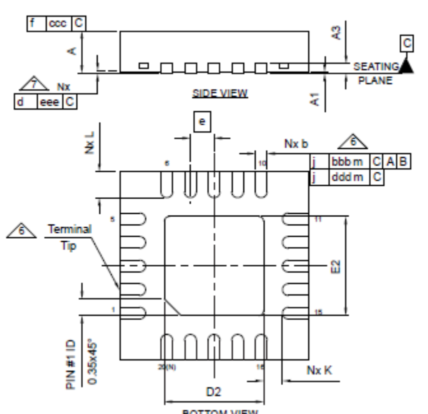

Table 24. QFN-20L 4.0 x 4.0 x 0.75 mm package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1		0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	3.95	4.00	4.05
D2	1.95	2.10	2.20
E	3.95	4.00	4.05
E2	1.95	2.10	2.20
e	0.50 BSC		
L	0.50	0.55	0.60
K	0.20		

DIMENSION	A	b	D	D2	E	E2	L
Data book **Min** (mm)	0.70	0.18	3.95	1.95	3.95	1.95	0.50
Data book **Typ** (mm)	0.75	0.25	4.00	2.10	4.00	2.10	0.55
Data book **Max** (mm)	0.80	0.30	4.05	2.20	4.05	2.20	0.60
1	0.75	0.258	4.015	2.107	4.023	2.122	0.551
2	0.746	0.259	4.015	2.108	4.023	2.117	0.556
3	0.754	0.258	4.016	2.107	4.022	2.118	0.549
4	0.742	0.257	4.018	2.107	4.021	2.122	0.549
5	0.752	0.255	4.016	2.107	4.02	2.119	0.548
6	0.754	0.26	4.017	2.105	4.02	2.119	0.546
7	0.751	0.258	4.017	2.108	4.02	2.118	0.561
8	0.748	0.258	4.018	2.109	4.021	2.12	0.544
9	0.759	0.256	4.016	2.108	4.02	2.123	0.548
10	0.756	0.257	4.017	2.109	4.023	2.12	0.548
11	0.744	0.257	4.018	2.107	4.02	2.119	0.548
12	0.753	0.256	4.017	2.105	4.021	2.123	0.547
13	0.747	0.254	4.018	2.107	4.019	2.121	0.548
14	0.751	0.258	4.016	2.108	4.019	2.121	0.546
15	0.752	0.258	4.018	2.109	4.02	2.118	0.554
16	0.749	0.258	4.019	2.106	4.021	2.12	0.545
17	0.759	0.258	4.018	2.105	4.023	2.122	0.545
18	0.747	0.258	4.018	2.105	4.02	2.12	0.545
19	0.751	0.259	4.017	2.104	4.02	2.123	0.551
20	0.756	0.258	4.016	2.105	4.022	2.121	0.551
MOY	**0.751**	**0.258**	**4.017**	**2.107**	**4.021**	**2.120**	**0.549**
MIN	**0.742**	**0.254**	**4.015**	**2.104**	**4.019**	**2.117**	**0.544**
MAX	**0.759**	**0.260**	**4.019**	**2.109**	**4.023**	**2.123**	**0.561**

6.3 Tests description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
SD Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.