PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/12/7104
Notification Date 02/21/2012

Front-End Capacity Extension for STripFET Technology - Grace Foundry (China)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	17-Feb-2012
Forecasted availabillity date of samples for customer	17-Feb-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	17-Feb-2012
Estimated date of changed product first shipment	22-May-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab process change
Reason for change	To optimize Power MOSFET productivity and ST's Wafer FAB utilization
Description of the change	Following the continuous improvement of our service and in order to rationalize and optimize Power MOSFET productivity, this document is announcing that STripFET Technology, currently manufactured in Ang Mo Kio (Singapore) Wafer FAB, will be also produced in the Grace Foundry (China) plant. STripFET Technology produced in Grace Foundry (China), guarantees the same quality and electrical characteristics as reported in the relevant data sheet. Devices used for qualification are available as Samples.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Internal codification, product marking, labelling and Q.A. number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt — **PCN IPD-PWR/12/7104**

Please sign and return to STMicroelectronics Sales Office — **Notification Date 02/21/2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Division Marketing Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

Dear Customer,

Please be informed that STripFET™ Technology, currently manufactured in Ang Mo Kio (Singapore) Wafer FAB, will be also produced in the Grace Foundry (China) plant.

The involved product series and affected Technologies are listed in the table below:

Product Family	Technology	Commercial Product / Series
Power MOSFET Transistors	STripFET™ V STripFET™ VI DeepGATE™	See attached list

Any other product related to the above table, even if not expressly included or partially mentioned in the attached list, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 07-2012.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power MOSFET Transistors	IPAK DPAK	STU60N3LH5 STD95N3LLH6

Change implementation schedule:

The first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power MOSFET Transistors	From Week 20-2012

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of STripFET™ Technology, manufactured in the Grace Foundry (China) plant, will be ensured by internal codification, product marking, labelling and Q.A. number.

Sincerely Yours.

Reliability Report On Front-End Capacity Extension for StripFET^{TM} Technology - Grace Foundry (China)

General Information	
Product Lines	5H33, 6L34
Product Description	N-Channel Power MOSFET
Commercial Products	STU60N3LH5 STD95N3LLH6
Product Group	IMS – IPD
Product division	Power Transistor Division
Package	IPAK/DPAK
Silicon Process technology	StripFET^{TM} Enhancement/DeepGate N-channel Power MOSFET

Locations	
Wafer fab	*Grace Foundry (China)*
Assembly plant	*ST Shenzhen (China)*
Reliability Lab	*IMS-IPD Catania Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	January 2012	8	C. Cappello	G. Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of Power MOSFET Transistors made in Grace Foundry (China).

3.2 Conclusion

The reliability tests have shown the good performances of the devices toward the environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Power MOSFET technology.

4.2 Construction note

D.U.T.: STU60N3LH5 LINE: 5H33 PACKAGE: IPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Grace Foundry (China)*
Technology	StripFET^{TM} Enhancement N-channel Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	2280 x 1730 μm^2
Metal	Al/Cu
Passivation type	No PASSIVATION

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	*ST Shenzhen (China)*
Package description	IPAK
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Gate Al 10 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*ST Shenzhen (China)*
Tester	IP TEST

D.U.T.: STD95N3LLH6 LINE: 6L34 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Grace Foundry (China)*
Technology	STripFET™ DeepGATE™ Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	2500 x 2200 μm^2
Metal	Al/Cu
Passivation type	No PASSIVATION

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	*ST Shenzhen (China)*
Package description	DPAK
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Gate Al 15 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*ST Shenzhen (China)*
Tester	IP TEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STU60N3LH5	5H33	Power MOSFET
2			Power MOSFET
3			Power MOSFET
1	STD95N3LLH6	6L34	Power MOSFET
2			Power MOSFET
3			Power MOSFET

5.2 Reliability test plan and results summary

D.U.T.: STU60N3LH5 LINE: 5H33 PACKAGE: IPAK

Test	Std ref.	Conditions	SS	Steps	Failure/SS	Note
HTRB	JESD22 A-108	TA = 175℃, V bias=24V	77 x 3 lots	1000 H	0/231	
HTGB	JESD22 A-108	Tj=150℃ , Vbias=20V	77 x 3 lots	1000 H	0/231	
AC	JESD22 A-102	Pa=2Atm / Ta=121℃	77 x 3 lots	96 H	0/231	
H3TRB	JESD22 A-101	TA=85℃ , RH=85% Vbias=30V	77 x 3 lots	1000 H	0/231	
HTSL	JESD22 A-103	Ta = 175℃	77 x 1 lot	1000H	0/77	
TC	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77 x 1 lot	500 cy	0/77	
TF / IOL	Mil-STD 750D Method 1037	ΔTc=+105℃ Pd=2 W	20 x 1 lot	10K cy	0/20	

D.U.T.: STD95N3LLH6 LINE: 6L34 PACKAGE: DPAK

Test	Std ref.	Conditions	SS	Steps	Failure/SS	Note
HTRB	JESD22 A-108	TA = 175℃, V bias=24V	77 x 3 lots	1000 H	0/231	
HTGB	JESD22 A-108	Tj=150℃ , Vbias=20V	77 x 3 lots	1000 H	0/231	
PC	JESD22 A-108	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	All devices to be submitted to H3TRB, TC, AC, IOL	-	0/559	
AC	JESD22 A-102	Pa=2Atm / Ta=121℃	77 x 3 lots	96 H	0/231	
H3TRB	JESD22 A-101	TA=85℃ , RH=85% Vbias=30V	77 x 3 lots	1000 H	0/231	
HTSL	JESD22 A-103	Ta = 175℃	77 x 1 lot	1000H	0/77	
TC	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77 x 1 lot	500 cy	0/77	
TF / IOL	Mil-STD 750D Method 1037	ΔTc=+105℃ Pd=2 W	20 x 1 lot	10K cy	0/20	

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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