PRODUCT/PROCESS CHANGE NOTIFICATION

PCN CRP/12/7013
Notification Date 01/24/2012

MATERIAL SET CHANGE for SO-8, SO-14 and SO-16 packages in ASE-Shangai introducing Copper Wire Bonding

Table 1. Change Implementation Schedule

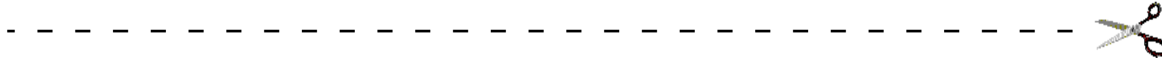
Forecasted implementation date for change	21-Mar-2012
Forecasted availabillity date of samples for customer	17-Jan-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	17-Jan-2012
Estimated date of changed product first shipment	24-Apr-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly material change
Reason for change	To improve service to ST Customers
Description of the change	To comply with the ST Roadmap aimed to rationalize the manufacturing processes and respond the ever increasing demand for the products housed in the packages in subject, ST is glad to announce the conversion to C.W.B. (Copper Wire Bonding) at the ASE-Shanghai (China) Subcontractor factory for : High Rel & Standard Products (P&L71) Voltage Regulators (P&L32)
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	see QA number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN CRP/12/7013**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 01/24/2012**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Vitali, Gian Luigi	Corporate Quality Manager
Cali, Paolo	Process Owner

WHAT:

To comply with the ST Roadmap aimed to rationalize the manufacturing processes and respond the ever increasing demand for the products housed in the packages in subject, ST is glad to announce the conversion to C.W.B. (Copper Wire Bonding) at the ASE-Shanghai (China) Subcontractor factory for:

Standard Products & HiRel
Linear Voltage Regulators & Voltage References

The ASE-Shanghai plant, will keep producing parts according to the ST Ecopack®2 (also called "Halogen Free") requirements for the packages in subject.

For the complete list of the part numbers affected by the change, please refer to the attached Products List.

Samples of test vehicles are available right now for immediate customer qualification, while other samples will be available upon request.

WHY:

To improve service to ST Customers;
To rationalize assembly processes;
To continue in the implementation of the Ecopack Program, the voluntary ST program to remove polluting and hazardous substances from all its products.

HOW:

By introducing C.W.B. manufacturing processes, according to the ST quality and reliability standard. The change here notified will not affect the electrical, dimensional and thermal parameters, keeping unchanged all information reported on the relevant product's datasheets.
There are no modifications in the packing modes or in the standard delivery quantities.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please, refer to Appendix 1 for all the details.

WHEN:

Production start and first shipments will occur as indicated in the table below.

Product Family	Production Start	1st Shipments
Standard Products & HiRel	From Week 15-2012	From Week 17-2012
Linear Voltage Regulators & Voltage References	From Week 15-2012	From Week 17-2012

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by the Q.A. number.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Reliability Evaluation Report

To qualify SOIC8L 1.0mils Cu wire in ASE SHANGHAI

T.V.: L78L05ACD-TR – Line: LA05

General Information	
Product Line	LA05
Product Description	Very low drop voltage regulators with inhibit
P/N	L78L05ACD-TR
Product Group	IMS, APM Group
Product division	IND.& POWER CONV Linear Voltage Regulators & Vref
Package	SO8
Silicon Process technology	C4 BIP (>6um)

Locations	
Wafer fab	AMKF : AMJ9 5"
Assembly plant	ASE SHANGHAI
Reliability Lab	**IMS-APM Catania Reliability Lab**

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	26-Sep-2011	9	Stefania Motta	Giovanni Presti	First Issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify SOIC8L 1.0mil Cu wire in ASE SHANGHAI-

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The L78Lxx series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat-sink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The L78Lxx series used as Zener diode/resistor combination replacement, offers an effective output impedance improvement.

4.2 Construction note

	P/N L78L05ACD-TR
Wafer/Die fab. information	
Wafer fab manufacturing location	AMJ9 5"
Technology	BIP (>6um)
Die finishing back side	LAPPED SILICON
Die size	1130,1270 UM
Bond pad metallization layers	1
Passivation type	SiN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac Singapore EWS 0899
Tester	QT200
Test program	LAXXEP**.CTS vers. E05
Assembly information	
Assembly site	ASE SHANGHAI(996M)
Package description	SOIC8L
Molding compound	**Hitachi CEL-9240HF10AK**
Frame material	COPPER 94X125MILS
Die attach process	Epoxy
Die attach material	Hitachi EN4900G
Die pad size	94x125 mils
Wire bonding process	Thermosonic Bonding
Wires bonding materials/diameters	1.0mil Cu wire
Final testing information	
Testing location	ASE SHANGHAI(996M)
Tester	ASL1000
Test program	LA05_ASE

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

6

Lot #	Diffusion Lot	Assy Lot	Package / Moldin Compound	Product Line	Comments
1	**W022EPX-Y**	**THM123N057**	SO8 / Hitachi CEL-9240HF10AK	LA05	1st Qual lot
2	**W022EPX-Y**	**THM124N015**	SO8 / Hitachi CEL-9240HF10AK	LA05	2nd Qual lot
3	**W022EPX-Y**	**THM125N026**	SO8 / Hitachi CEL-9240HF10AK	LA05	3rd Qual lot
4	**W022EPX-Y**	**THM123N058**	SO8 / Hitachi CEL-9240HF10AK	LA05	1e CORNER LOT HH
5	**W022EPX-Y**	**THM123N059**	SO8 / Hitachi CEL-9240HF10AK	LA05	2e CORNER LOT LL

6.1 Test plan and results summary

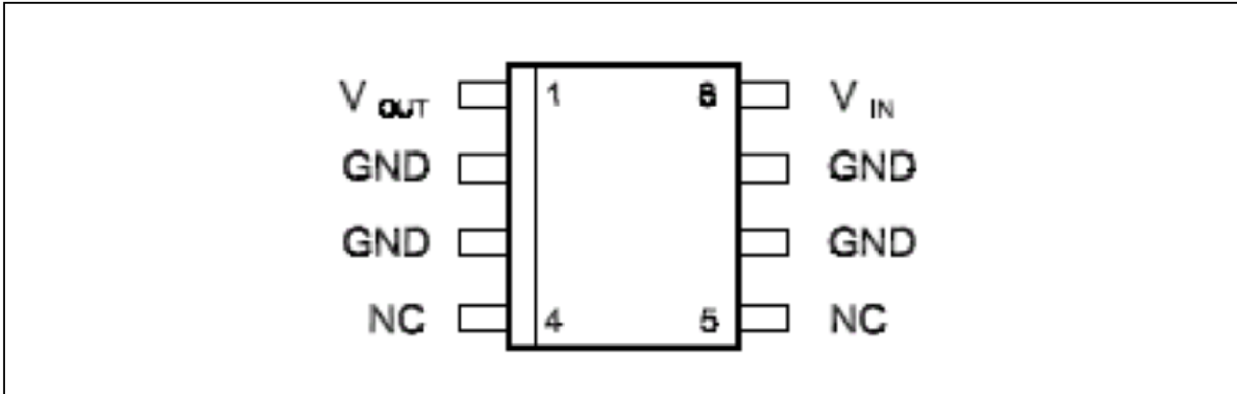
P/N L78L05ACD-TR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					note
						Lot 1 1°QUAL LOT	Lot 2 2°QUAL LOT	Lot 3 3°QUAL LOT	Lot 4 LOT HH	Lot 5 LOT LL	
Die Oriented Tests											
HTS	N	JESD22 A-103	Tj = 150°C	45	168 H	0/45	0/45	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	0/45	0/45	
HTS	N	JESD22 A-103	Tj = 175°C	45	168 H	0/45	0/45	0/45			Engineering Evaluation
					500 H	0/45	0/45	0/45			
					1000 H	0/45	0/45	0/45			
HTB	N	JESD22 A-108	Tj = 125°C, bias= +30V	77	168 H	0/77					
					500 H	0/77					
					1000 H	0/77					
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H	0/25	0/25	0/25			
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	0/25	0/25	0/25	0/25	
					300 cy	0/25	0/25	0/25	0/25	0/25	
					500 cy	0/25	0/25	0/25	0/25	0/25	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, bias= +24V		168 H	0/25	0/25	0/25			
					500 H	0/25	0/25	0/25			
					1000 H	0/25	0/25	0/25			

7 ANNEXES

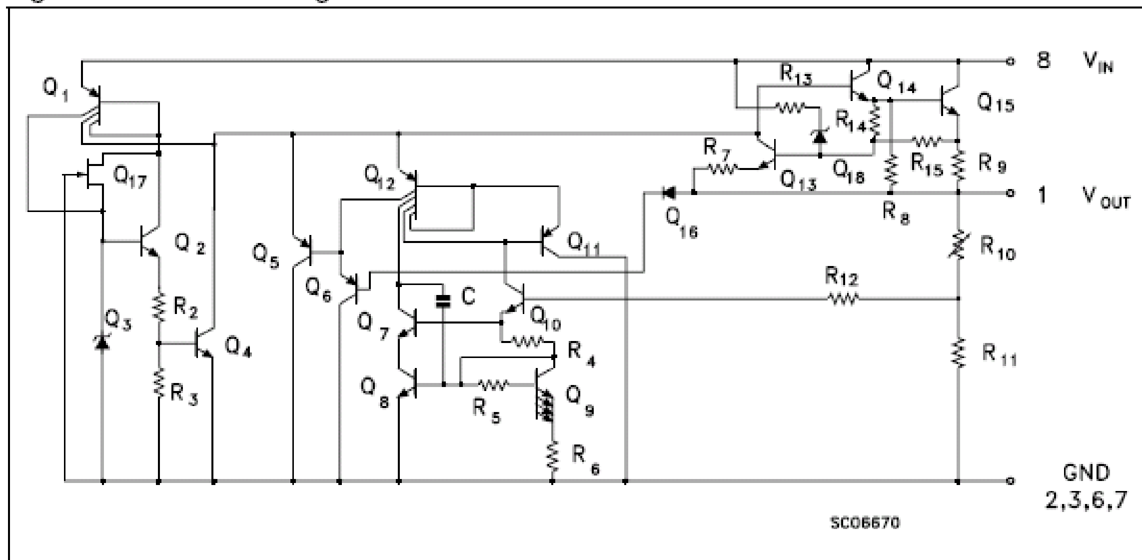
7.1 Device details

7.1.1 Pin connection



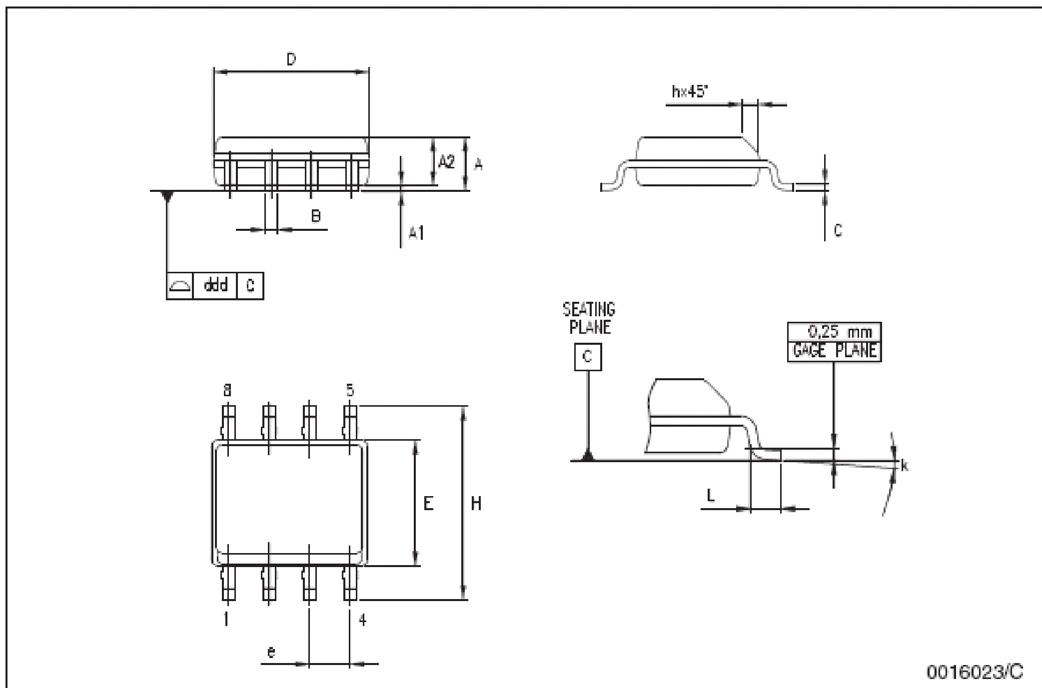
7.1.2 Block diagram

Figure 1. Schematic diagram



7.1.3 Package outline/Mechanical data

SO-8 mechanical data						
Dim.	**mm.**			**inch.**		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



7.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. g failure modes are "pop corn" and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moldingcompound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Reliability Report
Automotive Qualification

General Information	
Product Line	*0124*
Product Description	*General purpose Quad Op-Amps*
P/N	*LM324DT*
Product Group	*AMS*
Product division	*Analog*
Package	*SO14*
Silicon Process technology	*BIPOLAR / PRO450S-C*
Production mask set rev.	*0124BA REV 1*
Maturity level step	*from 10 to 30*

Locations	
Wafer fab	*AMK6 6"*
Assembly plant	*ASE Shanghai - CHINA*
Reliability Lab	*Grenoble*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	01-Dec-2011	11	Sebastien Gigandet	Jean-Marc Bugnard	First issue

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6.2 TESTS DESCRIPTION 10

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the copper wire for SO Narrow produced in ASE Shanghai for Hirel & standard products.
The test Vehicle is the 0124 line in PRO Bipolar technology.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the device behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

LM124, LM224, LM324

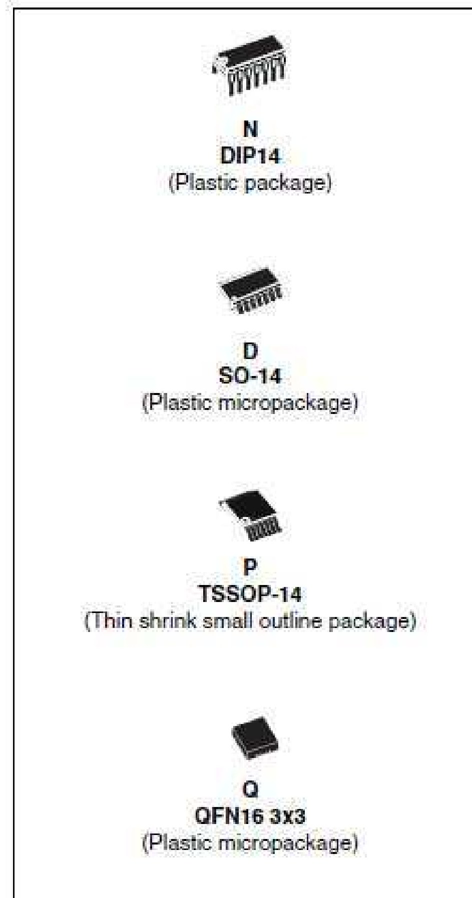
Low power quad operational amplifiers

Features

- Wide gain bandwidth: 1.3 MHz
- Input common-mode voltage range includes ground
- Large voltage gain: 100 dB
- Very low supply current per amplifier: 375 µA
- Low input bias current: 20 nA
- Low input offset voltage: 5 mV max.
- Low input offset current: 2 nA
- Wide power supply range:
  - Single supply: +3 V to +30 V
- Dual supplies: ±1.5 V to ±15 V

Description

The LM124, LM224 and LM324 consist of four independent, high gain, internally frequency-compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.



4.2 Construction note

	P/N *LM324DT*
Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6
Technology	BIPOLAR
Process family	PRO450S-C
Die finishing back side	RAW SILICON - BACK GRINDING
Die size	1430,1360 UM
Bond pad metallization layers	AlSiCu
Passivation type	SiN (nitride)
Poly silicon layers	NA
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac Singapore
Tester	ASL1000
Test program	T0124AW
Assembly information	
Assembly site	ASE Shanghai - CHINA
Package description	SO 14
Molding compound	Hitachi CEL-9240HF10AK
Frame material	L/F 90*120 (2.286*3.048) Copper + Ag spot
Die attach process	Glue Attach
Die attach material	Hitachi EN4900G
Die pad size	80,80 UM
Wire bonding process	Wire Bonder
Wires bonding materials/diameters	Copper Wire 1 mils
Lead finishing process	Plating
Lead finishing/bump solder material	Sn
Substrate supplier for BGA	NA
Final testing information	
Testing location	ASE Shanghai - CHINA
Tester	ASL1000
Test program	T0124BF

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	W123FJJ	11020016380	G0129022	SO14	0124	
2						
3						

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

P/N LM324DT

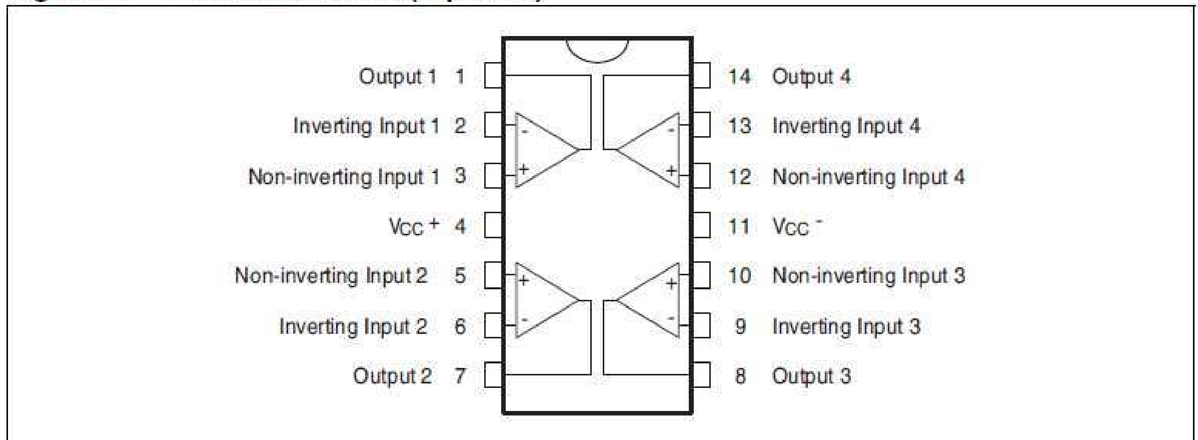
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Lot 2	Lot 3	Note
Die Oriented Tests									
HTSL	N	JESD22 A-103	Ta = 150℃	78	168 H	0/78			
					500 H	0/78			
					1000 H	0/78			
Package Oriented Tests									
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	78	96 H	0/78			
					168 H	0/78			
TC	Y	JESD22 A-104	Ta = -65℃ to 150 ℃	78	100 cy	0/78			
					500 cy	0/78			
					1000 cy	0/78			

6 ANNEXES

6.1 Device details

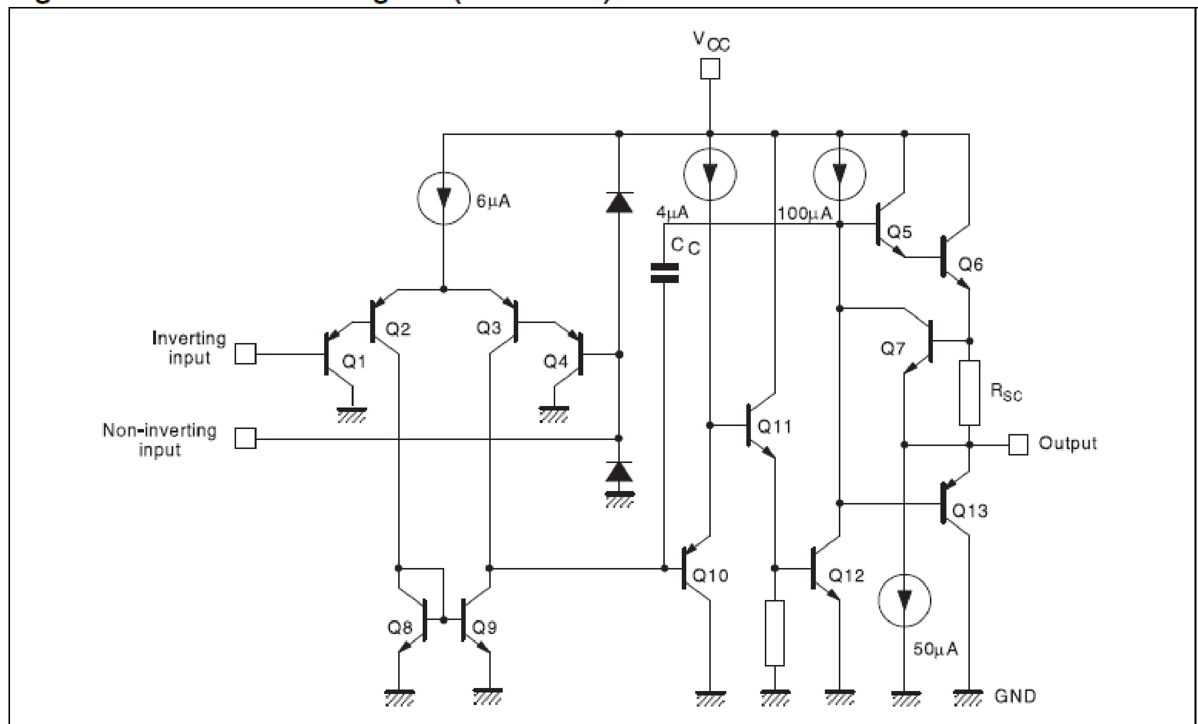
6.1.1 Pin connection

Figure 1. Pin connections (top view)

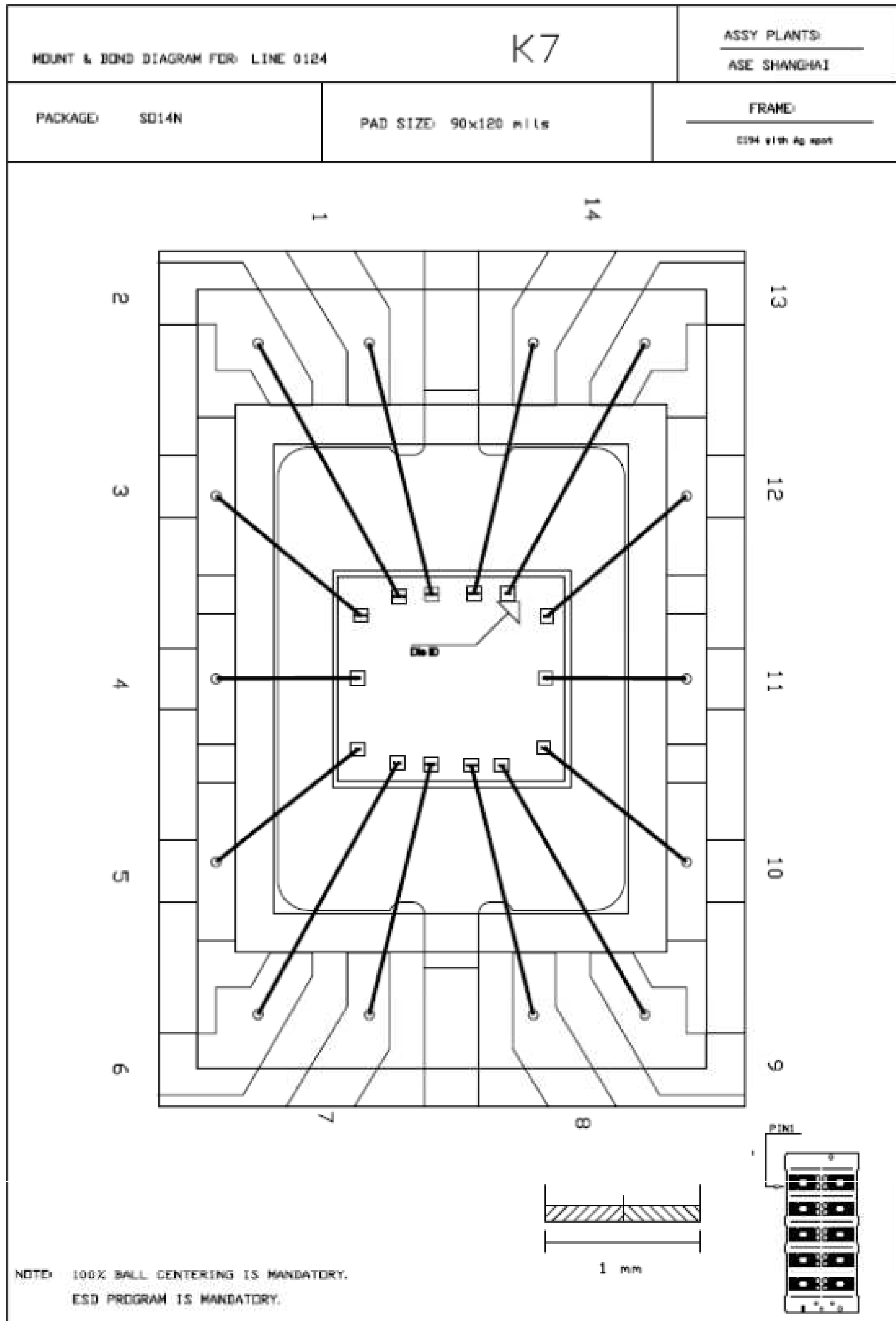


6.1.2 Block diagram

Figure 2. Schematic diagram (1/4 LM124)



6.1.3 Bonding diagram



6.1

Figure 29. SO-14 package mechanical drawing

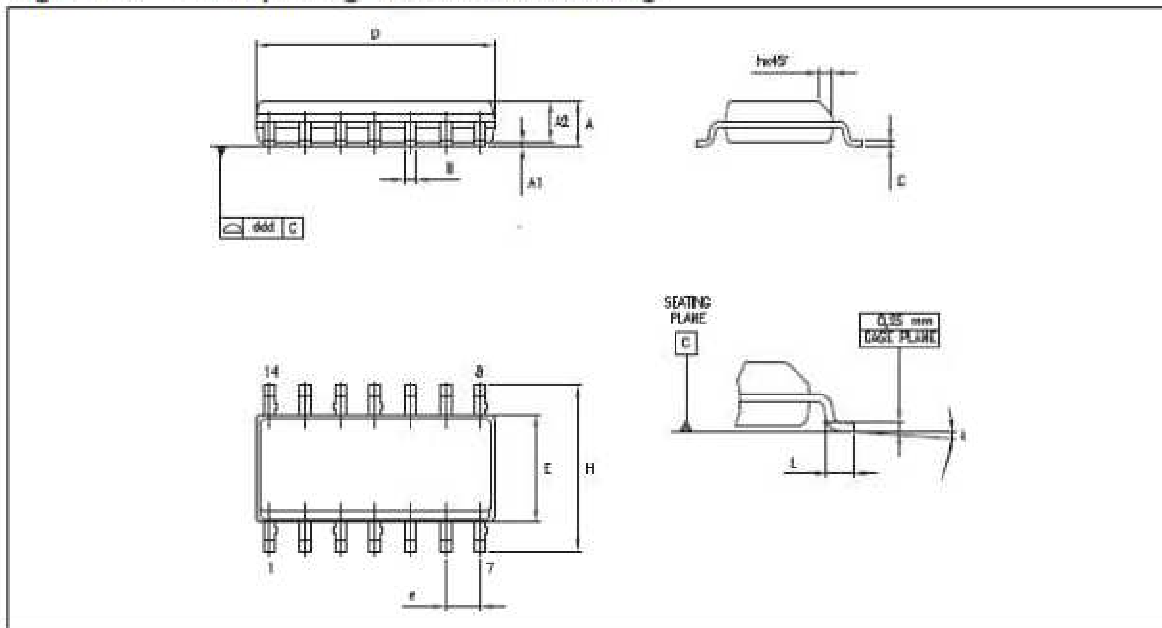


Table 4. SO-14 package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in ai atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Reliability Report

To qualify SOIC16L Cu wire in ASE SHANGHAI

T.V.:ULQ2003D1R – L203CAW line

General Information	
Product Line	L203
Product Description	Seven Darlington array
P/N	ULQ2003D1R
Product Group	APM (Voltage regulator & Interface) Group
Product division	IND.& POWER CONV.
Package	SO16
Silicon Process technology	C4 BIP (>6UM)
Production mask set rev.	22078

Locations	
Wafer fab	*AMKF : AMJ9 5"*
Assembly plant	*ASE SHANGHAI*
Reliability Lab	*Reliability Lab. Site Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	26-Sep-2011	8	Angelo Basile Giuseppe Failla	Giovanni Presti	Final

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify SOIC16L Cu wire in ASE SHANGHAI.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The ULQ2001, ULQ2003 and ULQ2004 are high voltage, high current Darlington arrays each containing seven open collector Darlington pairs with common emitters. Each channel rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout. The versions interface to all common logic families. These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal print-heads and high power buffers. The ULQ2001A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO16) as ULQ2003D1/2004D1. The ULQ2003 is available as Automotive Grade in SO16 package.

4.2 Construction note

	P/N ULQ2003D1013TRY
Wafer/Die fab. information	
Wafer fab manufacturing location	AMKF : AMJ9 5"
Technology	C4 BIP (>6um)
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	2340,1300 UM
Passivation type	SiN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac Singapore EWS 0899
Tester	TESTER A360
Test program	L203SZ07
Assembly information	
Assembly site	ASE SHANGHAI
Package description	SO16
Molding compound	Hitachi CEL-9240HF
Frame material	C194 with Ag spot 120 x 90mils
Die attach process	Epoxy
Die attach material	Hitachi EN4900G
Die pad size	120 x 90mils
Wire bonding process	Thermosonic Bonding
Wires bonding materials/diameters	1.0mils Cu wire
Lead finishing process	Pure Tin Plating Sn 100%
Final testing information	
Testing location	ASE SHANGHAI
Tester	ASL1000
Test program	L203_ASE_01.prg

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot	Diffusion Lot	Assy Lot	Process/ Package	Product Line	Comments
1	W045EET	THM123N060	SOIC16L	L203	Final

5.2 Test plan and results summary

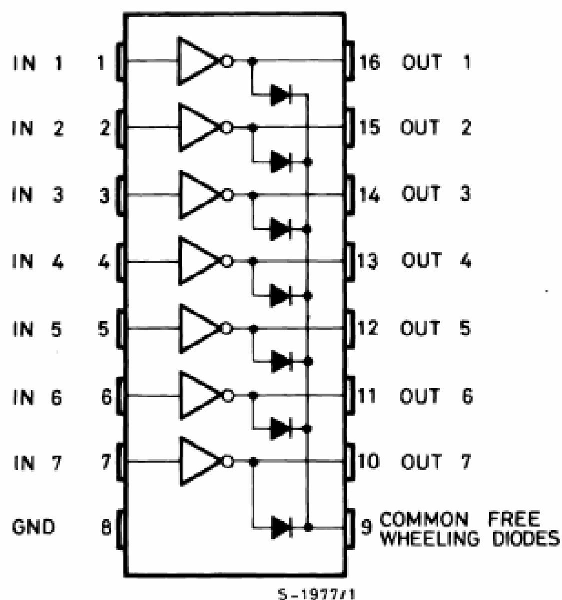
P/N ULQ2003D1R

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Lot 2	Lot 3	Corner HH	Corner LL	Note
Die Oriented Tests											
HTB	N	JESD22 A-108	Tj = 125℃, Vcc= +50V	77	168 H	0/77					
					500 H	0/77					
					1000 H	0/77					
HTSL	N	JESD22 A-103	Ta = 150℃	135	168 H	0/45	0/45	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	0/45	0/45	
HTSL	N	JESD22 A-103	Ta = 175℃	135	168 H	0/45	0/45	0/45	0/45	0/45	Engineering evaluation
					500 H	0/45	0/45	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	0/45	0/45	
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 40 H @ Ta=60℃ Rh=60% Oven Reflow @ Tpeak=260℃ 3 times	500	Final	Pass	Pass	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	75	168 H	0/25	0/25	0/25			
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃	125	100 cy	0/25	0/25	0/25	0/25	0/25	
					200 cy	0/25	0/25	0/25	0/25	0/25	
					500 cy	0/25	0/25	0/25	0/25	0/25	
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, Vcc= +40V	125	168 H	0/25	0/25	0/25	0/25	0/25	
					500 H	0/25	0/25	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	0/25	0/25	

6 ANNEXES

6.1 Device details

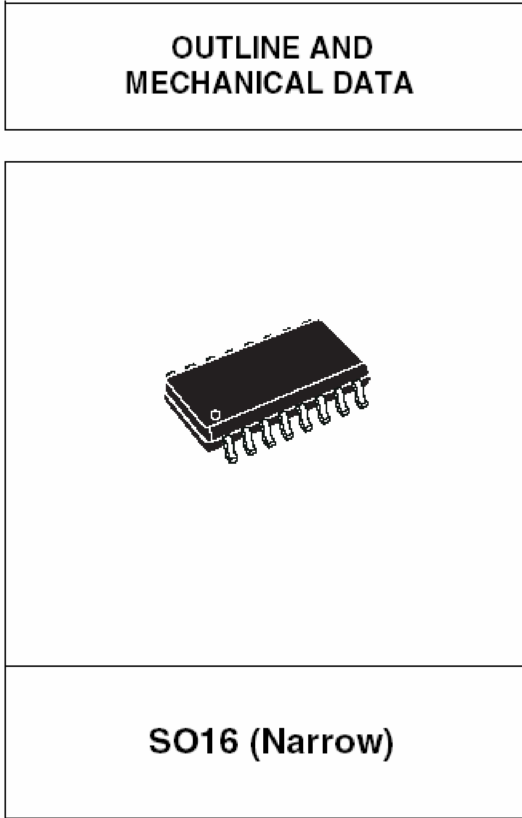
6.1.1 Pin connection

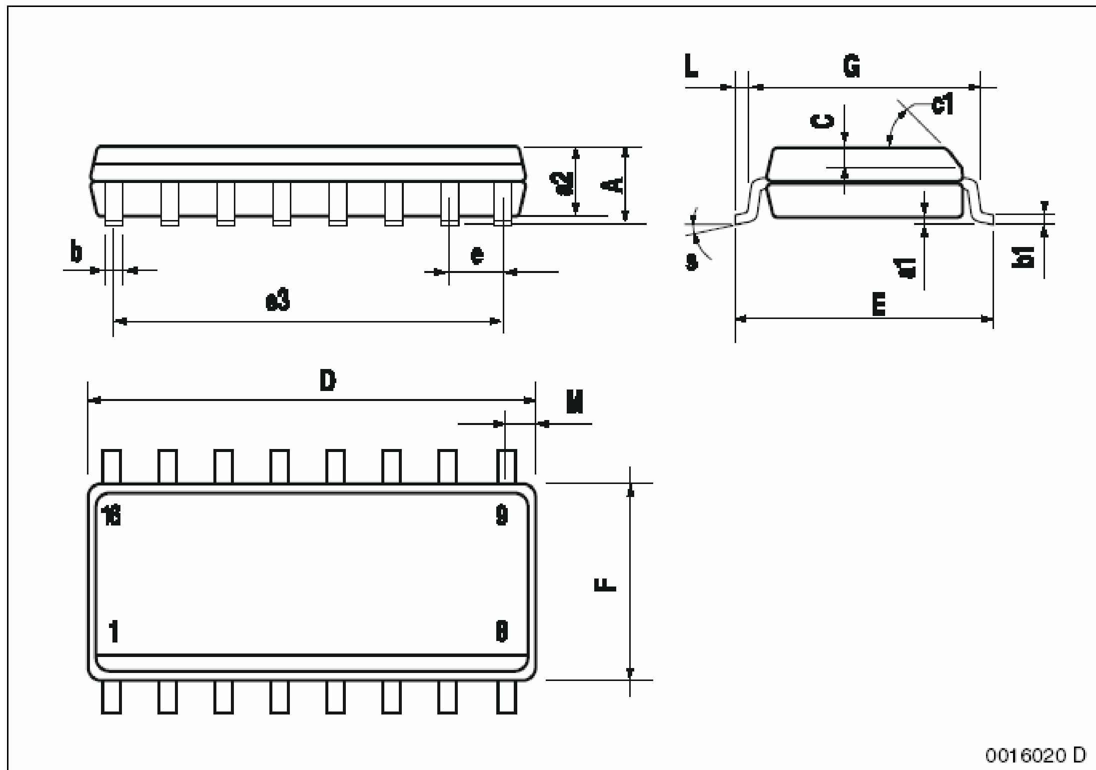


6.1.2 Package outline/Mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 ° (max.)					

(1) "D" and "F" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.006inc.)





6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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Reliability Report

T.V.: HCF4093M013TR – P93B
Cu Wires – SO14 – ASE SHANGHAI Plant

General Information	
Product Line	*P93B01*
Product Description	*QUAD 2 INPUT NAND SCHMITT TRIGGER*
P/N	*HCF4093M013TR*
Product Group	*APM*
Product division	*3M MEMS, SENSOR & HIGH PERF. ANALOG*
Package	*SO14L*
Silicon Process technology	*CMOSMG*

Locations	
Wafer fab	*Singapore AMK -Jetmos-*
Assembly plant	*ASE Assembly & Test (Shanghai)*
Reliability Lab	*Reliability Lab Site Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	27-Oct-2011	7	Angelo Basile Giuseppe Failla	Giovanni Presti	Final

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
AEC-Q100	Stress test qualification for automotive grade integrated circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify SOIC14L 1 Mils Cu wire in ASE SHANGHAI.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The HCF4093 is a monolithic integrated circuitfabricated in metal oxide semiconductor technology available in DIP and SOP packages.The HCF4093 type consists of 4 schmitt trigger circuits. Each circuit functions has a 2-inputNAND gate with schmitt trigger action on both inputs. The gate switches at different points forpositive and negative going signals. The difference between the positive voltage (VP) andthe negative voltage (VN) is defined as hysteresis voltage (VH).

4.2 Construction note

	P/N P93BCWB
Wafer/Die fab. information	
Wafer fab manufacturing location	0857 Singapore AMK -Jetmos
Technology	MOS
Die finishing back side	RAW SILICON
Die size	1484x0.933mm2
Passivation type	P-VAPOX(SiO2) / NITRIDE (SiN)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac EWS 0899
Tester	CTS600
Test program	C4093E2
Assembly information	
Assembly site	996M ASE Assembly & Test (Shanghai)
Package description	K7 (SOIC-14)
Molding compound	Hitachi CEL-9240HF10AK
Frame material	L/F 90*120 (2.286*3.048) Copper + Ag spot
Die attach material	D/A Hitachi EN4900G
Wires bonding materials/diameters	Wire 1 mils Copper (pd coated)
Final testing information	
Testing location	Z6MT (996M)
Tester	ASL1K/8T861
Test program	P93BUA10A11

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Process/ Package	Product Line	Comments
1	W123FJJ	SO14	P93B	Final

5.2 Test plan and results summary

P/N HCF4093M013TR

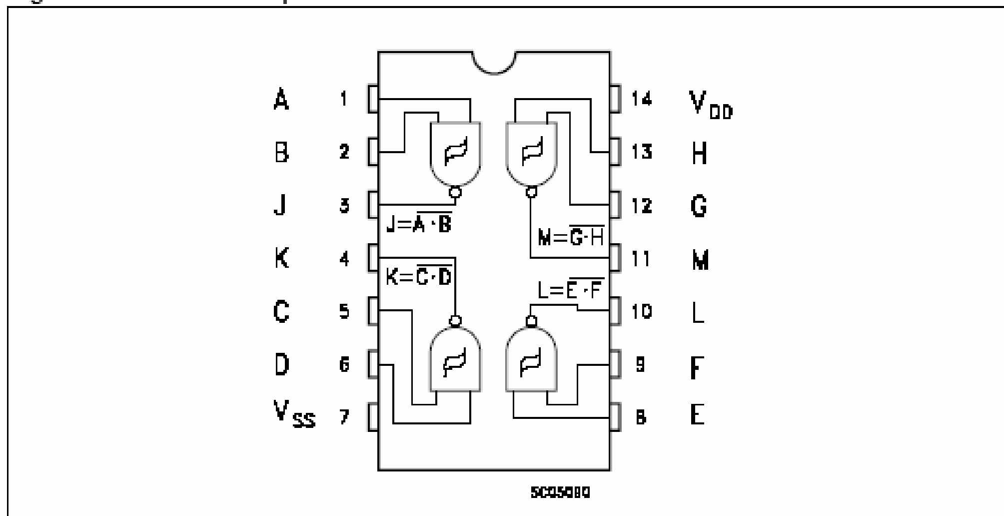
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
Die Oriented Tests							
HTSL	N	JESD22 A-103	Ta = 175℃	45	168 H	0/45	
					500 H	0/45	
					1000 H	0/45	
HTSL	N	JESD22 A-103	Ta = 150℃	45	168 H	0/45	
					500 H	0/45	
					1000H	0/45	
HTB	N	JESD22 A-108	Tj = 125C, BIAS +22V	77	168 H	0/77	
					500 H	0/77	
					1000H	0/77	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260C 3 times		Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	77	168H	0/77	
TC	Y	JESD22 A-104	Ta = -65C to 150 ℃	77	100 cy	0/77	
					300 cy	0/77	
					500 cy	0/77	
THB	Y	JESD22 A-101	Ta =85C, RH =85%, BIAS=+16V	77	168 H	0/77	
					500 H	0/77	
					1000h	0/77	

6 ANNEXES

6.1 Device details

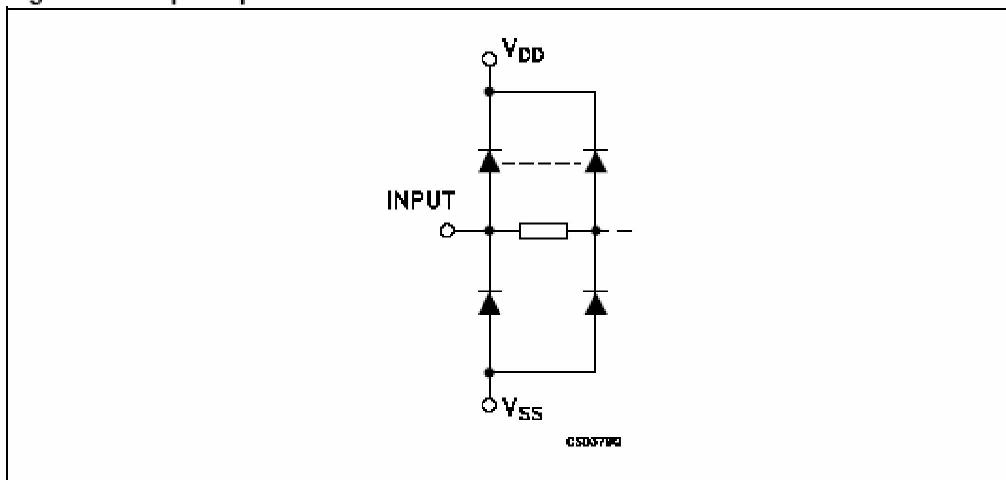
6.1.1 Pin connection

Figure 1. HCF4093B pin connection



6.1.2 Block diagram

Figure 2. Input equivalent circuit



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
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Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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